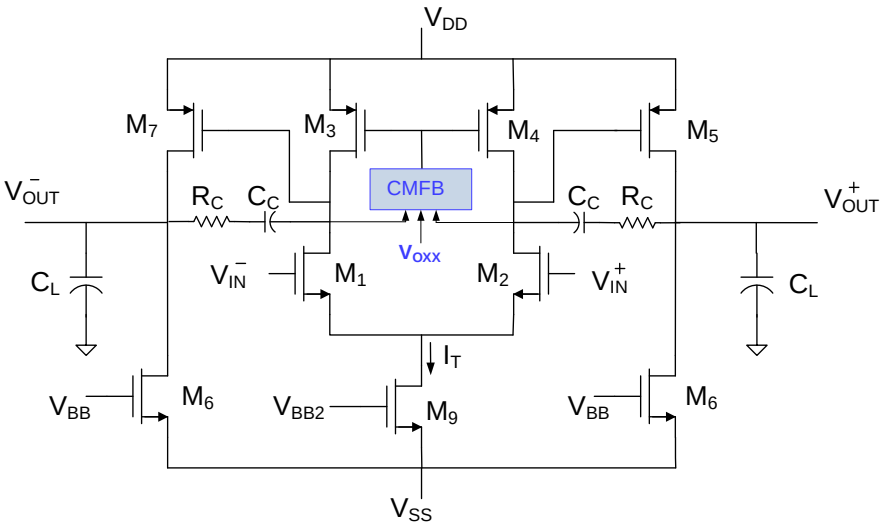
EE 435

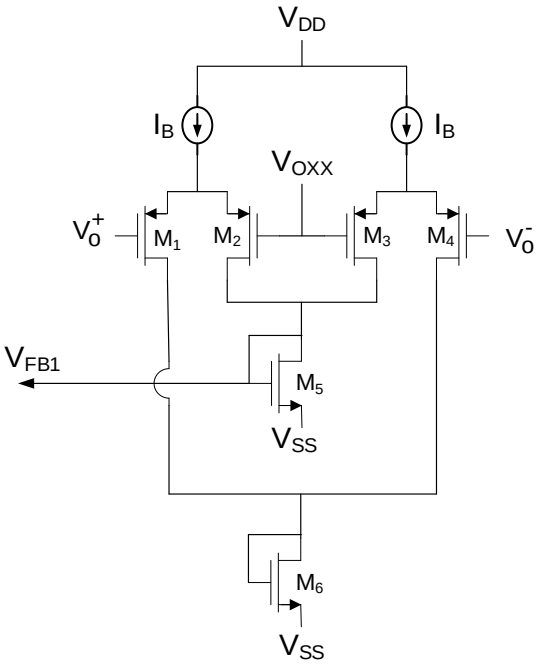
Lecture 32

String DACs

Laboratory Support



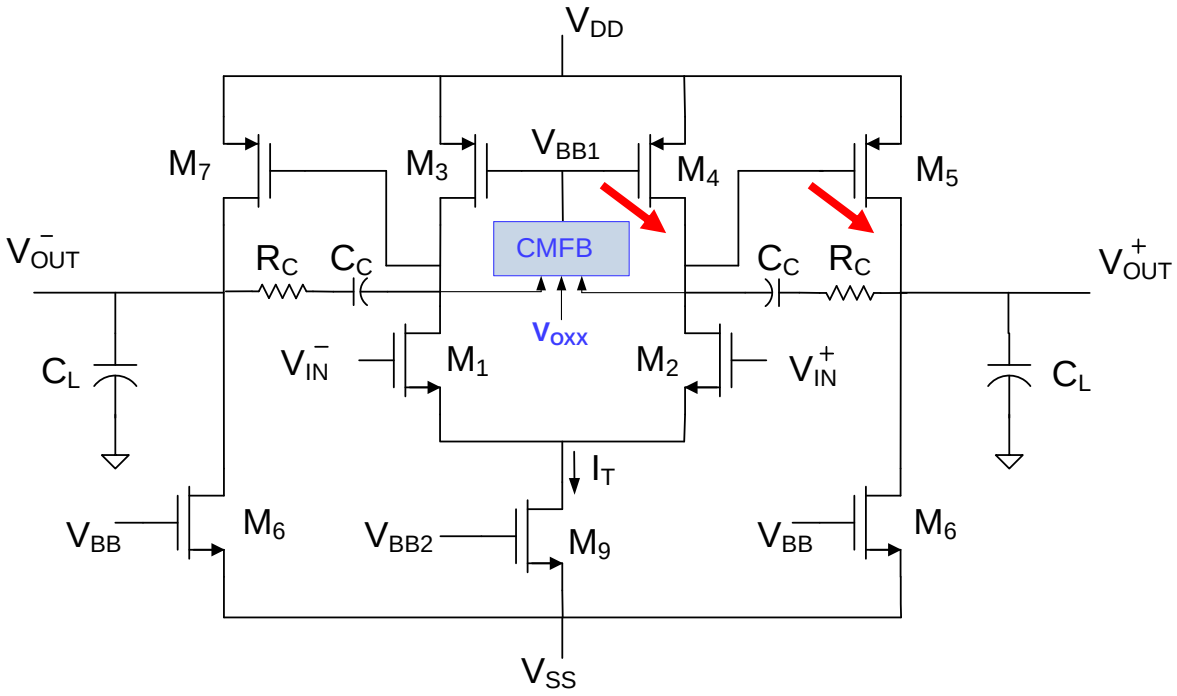
Two-Stage Fully Differential Op Amp



A continuous-time CMFB Circuit

Must have negative feedback to control biasing of first stage of Op Amp

Laboratory Support



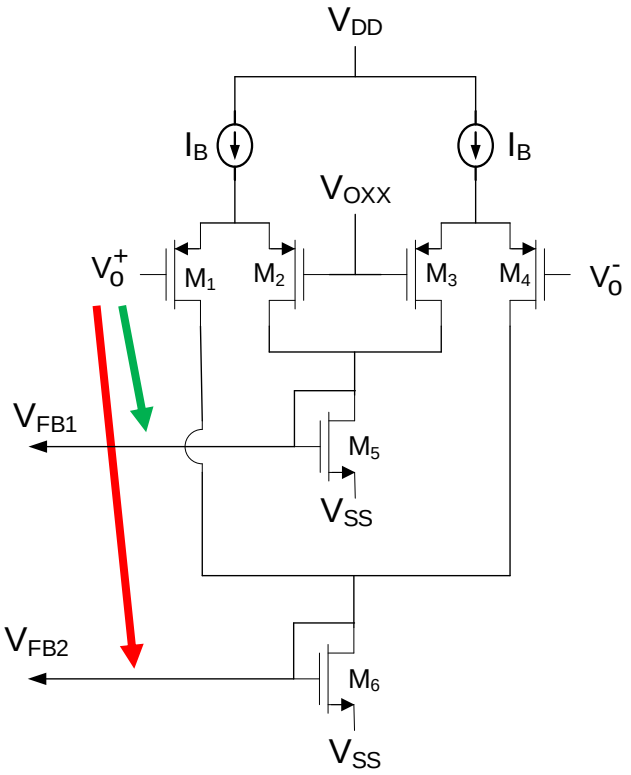
Must have negative feedback to control biasing of first stage of Op Amp

Can provide feedback to either V_{BB1} or V_{BB2} (feedback to V_{BB1} depicted)

Two inversions from either V_{BB1} or V_{BB2} in this op amp

Need one more inversion in sample CMFB

Laboratory Support

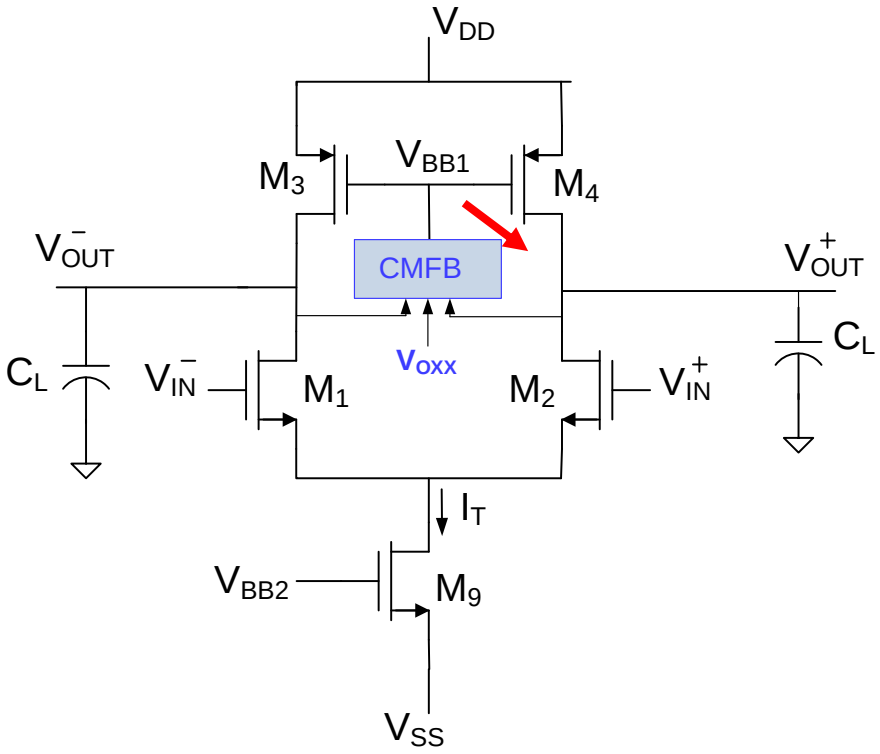


Must have negative feedback to control biasing of first stage of Op Amp

One inversion to V_{FB2}

No Inversions to V_{FB1}

Laboratory Support



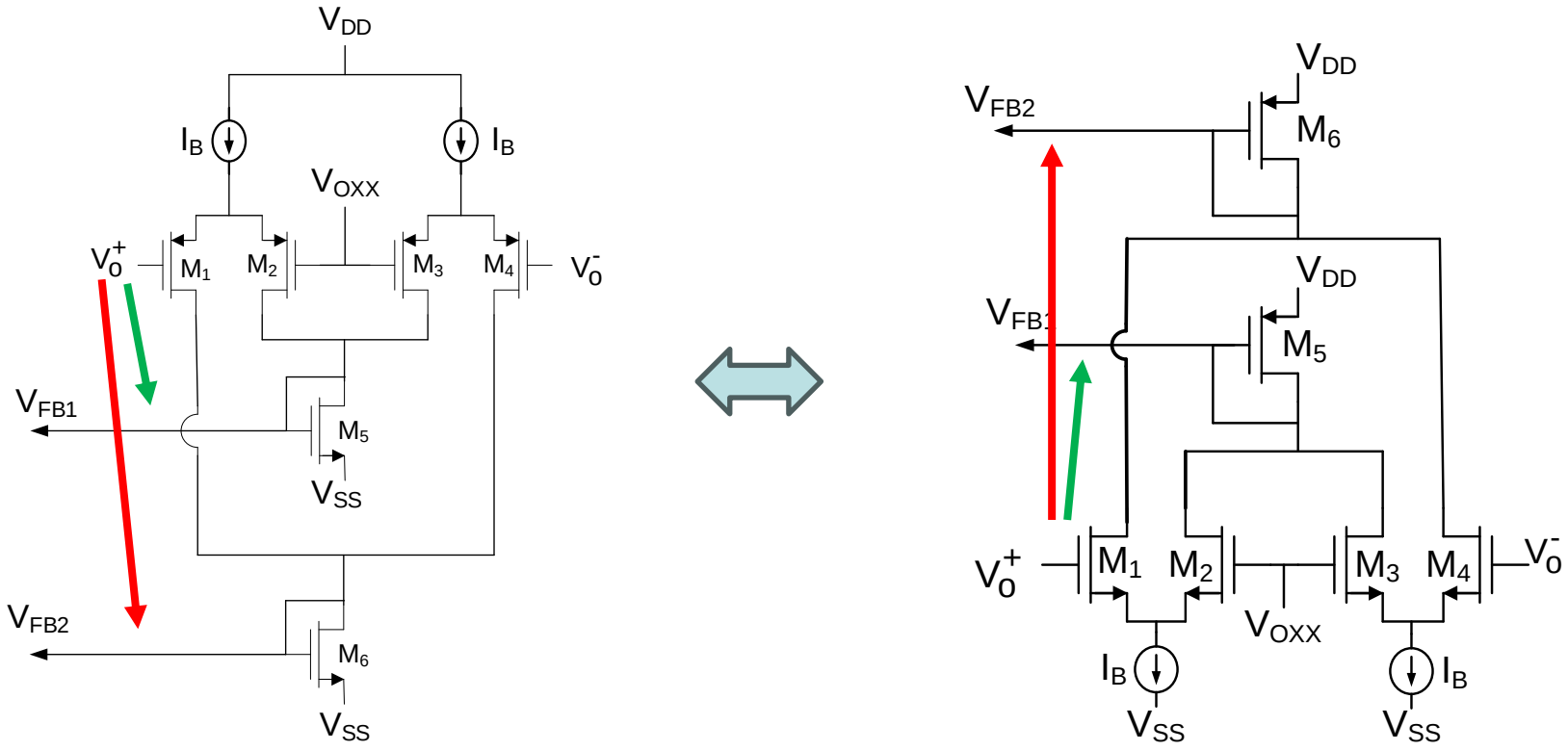
Must have negative feedback to control biasing of first stage of Op Amp

Can provide feedback to either V_{BB1} or V_{BB2} (feedback to V_{BB1} depicted)

One inversions from either V_{BB1} or V_{BB2} in this op amp

Want no inversions in sample CMFB circuit

Laboratory Support

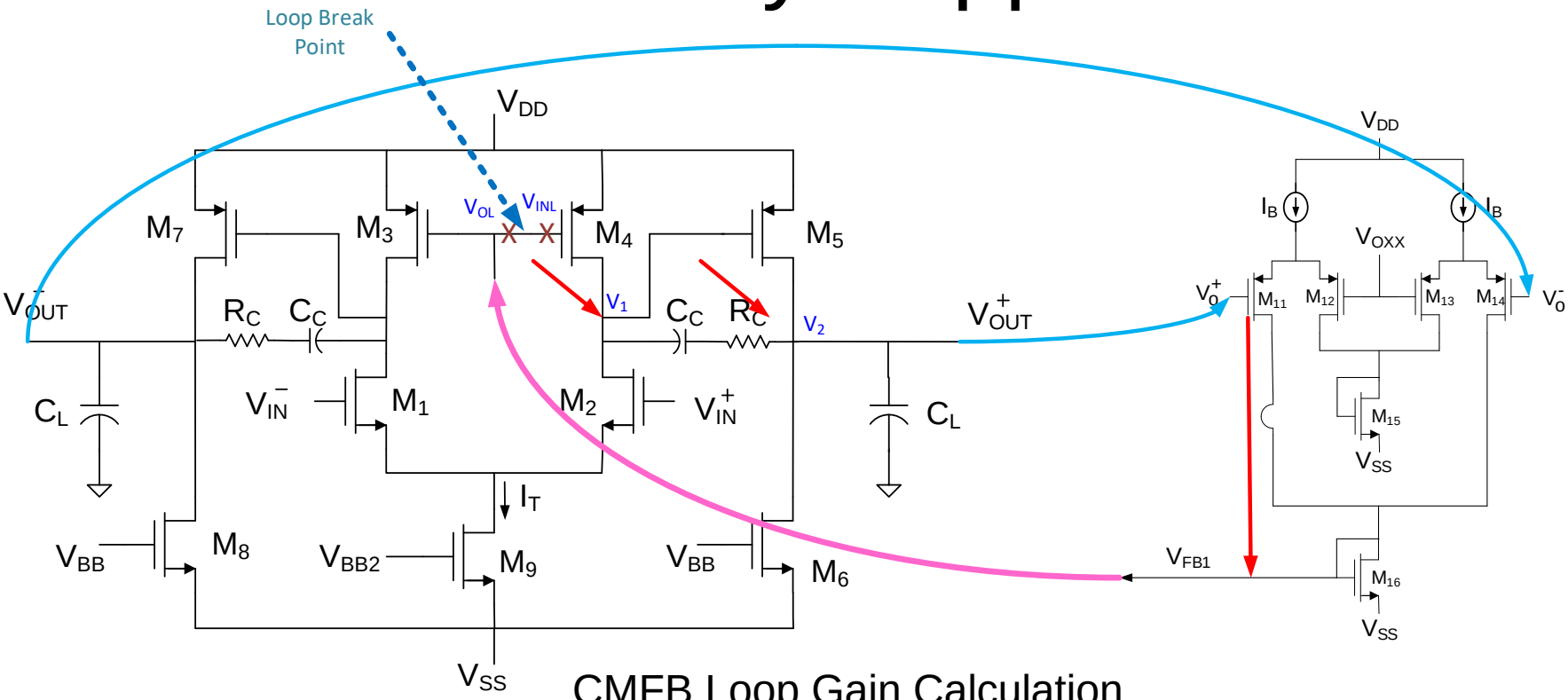


Counterpart Circuit

Must have negative feedback to control biasing of first stage of Op Amp

Small-signal performance (small-signal domains) are the same
Circuit or Counterpart May Have Preferrable Bias Voltage Levels

Laboratory Support



CMFB Loop Gain Calculation

$$\frac{V_{OL}}{V_{INL}} = \frac{V_1}{V_{INL}} \frac{V_2}{V_1} \frac{V_{OL}}{V_2}$$

$$\frac{V_1}{V_{INL}} = \frac{-g_{m4}}{g_{04} + \tilde{g}_{O9} \dfrac{g_{02}}{g_{m2}}} \simeq \frac{-g_{m4}}{g_{04}}$$

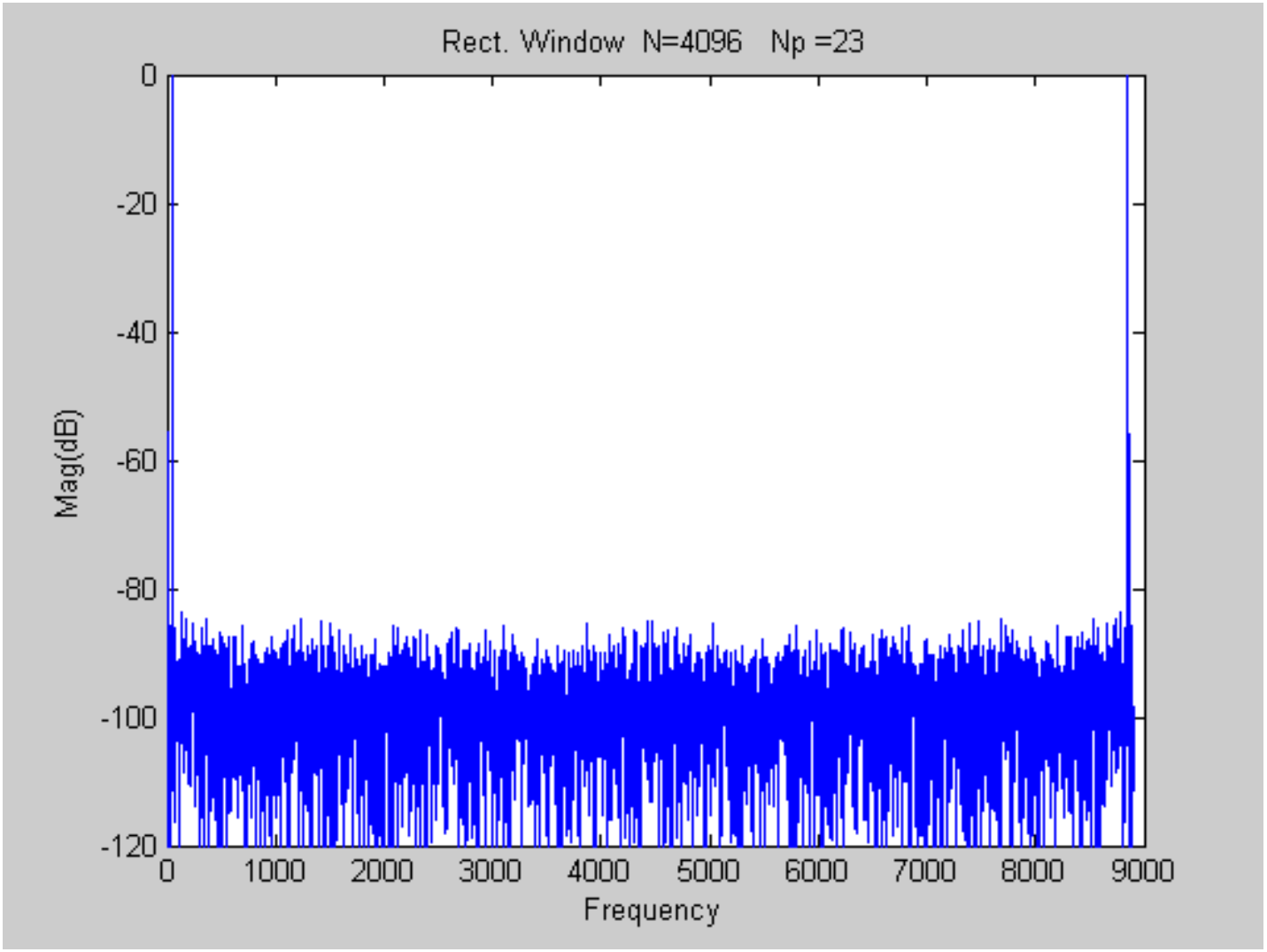
$$\frac{V_2}{V_1} = \frac{-g_{m5}}{g_{05} + g_{06}} \simeq \frac{-g_{m5}}{2g_{05}}$$

$$\frac{V_{OL}}{V_2} = \frac{-\left(\dfrac{g_{m11}}{2} + \dfrac{g_{m14}}{2}\right)}{g_{m16} + g_{o16} + g_{011} + g_{012}} \simeq \frac{-g_{m11}}{g_{m16}}$$

$$\frac{V_{OL}}{V_{INL}} = -\frac{g_{m4}}{g_{04}} \frac{g_{m5}}{2g_{05}} \frac{g_{m11}}{g_{m16}}$$

Quantization Effects

Res = 10 bits



Note at higher resolution the DFT terms due to quantization are quite flat

Summary of time and amplitude quantization assessment

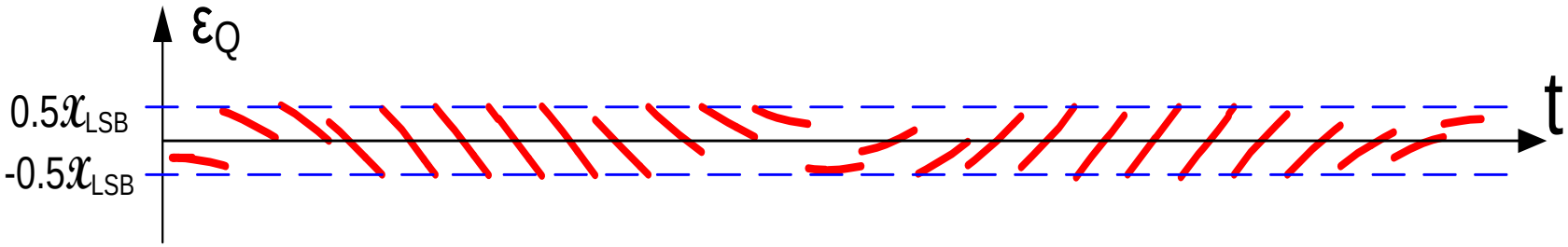
Time and amplitude quantization do not introduce harmonic distortion

Time and amplitude quantization do increase the noise floor

Will analytically determine “Quantization Noise” in next lecture

Quantization Noise in ADC

How does the SNR change if the input is a sinusoid that goes from 0 to x_{REF} centered at $x_{REF}/2$?



For low f_{SIG}/f_{CL} ratios, bounded by $\pm 0.5\ X_{LSB}$ and at any point in time, behaves almost as if a uniformly distributed random variable

$$\varepsilon_Q \sim U[-0.5X_{LSB}, 0.5X_{LSB}]$$

Quantization Noise in ADC

Recall:

If the random variable f is uniformly distributed in the interval [A,B]
f : U[A,B] then the mean and standard deviation of f are given by

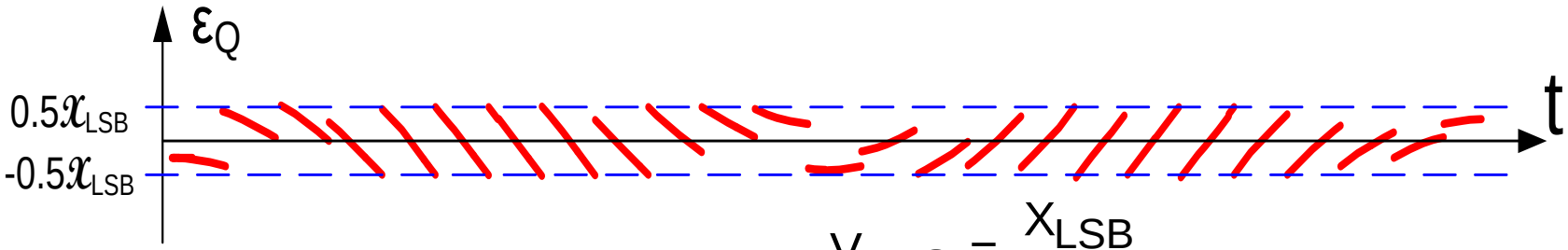
$$\mu_f = \frac{A+B}{2} \qquad \sigma_f = \frac{B-A}{\sqrt{12}}$$

Theorem: If n(t) is a random process and $\langle n(kT_S) \rangle$ is a sequence of samples of n(t) then for large T/T_S,

$$V_{RMS} = \sqrt{\frac{1}{T}\int_{t_1}^{t_1+T} n^2(t)\,dt} = \sqrt{\sigma^2_{n(kT_S)} + \mu^2_{n(kT_S)}}$$

Quantization Noise in ADC

How does the SNR change if the input is a sinusoid that goes from 0 to x_{REF} centered at $x_{REF}/2$?



$$V_{RMS} = \frac{X_{LSB}}{\sqrt{12}}$$

But $$V_{INRMS} = \left(\frac{X_{REF}}{2}\right)\frac{1}{\sqrt{2}}$$

Thus obtain

$$SNR = \frac{\frac{X_{REF}}{2\sqrt{2}}}{\frac{X_{LSB}}{\sqrt{12}}} = 2^n\sqrt{\frac{3}{2}}$$

Finally, in db,

$$SNR_{dB} = 20\log\left(2^n\sqrt{\frac{3}{2}}\right) = 6.02\,n + 1.76$$

ENOB Summary

Resolution:

$$\text{ENOB} = \frac{\log_{10} N_{ACT}}{\log_{10} 2} = \log_2 N_{ACT}$$

INL:

$$\text{ENOB} = n_R - \log_2(\upsilon) - 1$$

n_R specified res, v INL in LSB

DNL:

$$\text{ENOB} = \log_2\left(1 + \left(\frac{V_{MAX} - V_{MIN}}{\Delta_{MAX}}\right)\right)$$

V_{MAX} and V_{MIN} are max and min outputs and Δ_{MAX} is maximum absolute step (HW problem)

Quantization noise:

$$\text{ENOB} = \frac{SNR_{dB}}{6.02}$$

rel to triangle/sawtooth

$$\text{ENOB} = \frac{SNR_{dB} - 1.76}{6.02}$$

rel to sinusoid

Absolute Accuracy

Absolute Accuracy is the difference between the actual output and the ideal or desired output of a data converter

The ideal or desired output is in reference to an absolute standard (often maintained by the National Institute of Standards and Technology (NIST) formerly Bureau of Standards) and could be volts, amps, time, weight, distance, or one of a large number of other physical quantities)

Absolute accuracy provides no tolerance to offset errors, gain errors, nonlinearity errors, quantization errors, or noise

In many applications, absolute accuracy is not of a major concern

but … scales, meters, etc. may be more concerned about Absolute accuracy than any other parameter

Relative Accuracy

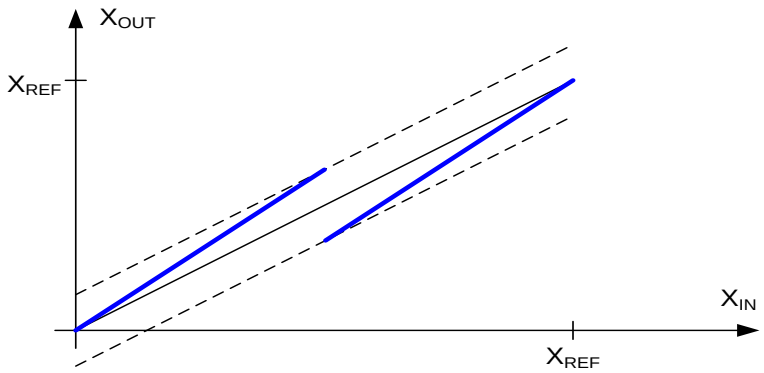
In the context of data converters, pseudo-static Relative Accuracy is the difference between the actual output and an appropriate fit-line to overall output of the data converter

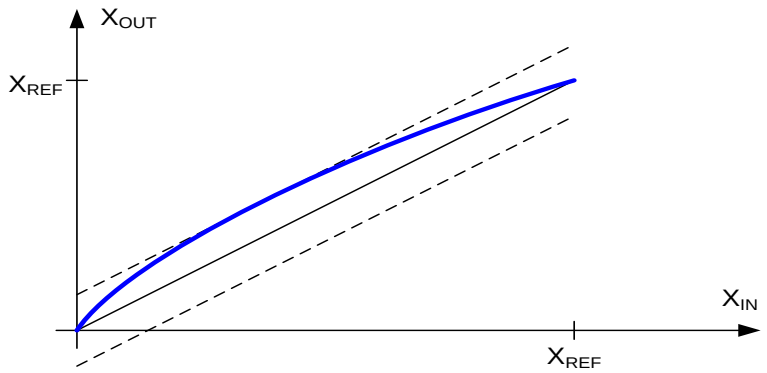
INL is often used as a measure of the relative accuracy

In many, if not most, applications, relative accuracy is of much more concern than absolute accuracy

Some architectures with good relative accuracy will have very small deviations in the outputs for closely-spaced inputs whereas others may have relatively large deviations in outputs for closely-spaced inputs

DNL provides some measure of how outputs for closely-spaced inputs compare





Performance Characterization of Data Converters

Static Characteristics

Dynamic Characteristics

Have spent several lectures discussing Static Characteristics

Dynamic Characteristics are also important but due to time limitations will not be discussed in detail in this course

Performance Characterization of Data Converters

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Low-f Spurious Free Dynamic Range (SFDR)
  - Low-f Total Harmonic Distortion (THD)
  - Effective Number of Bits (ENOB)
  - Power Dissipation

Performance Characterization of Data Converters

- Dynamic characteristics
  - Conversion Time or Conversion Rate (ADC)
  - Settling time or Clock Rate (DAC)
  - Sampling Time Uncertainty (aperture uncertainty or aperture jitter)
  - Dynamic Range
  - Spurious Free Dynamic Range (SFDR)
  - Total Harmonic Distortion (THD)
  - Signal to Noise Ratio (SNR)
  - Signal to Noise and Distortion Ratio (SNDR)
  - Sparkle Characteristics
  - Effective Number of Bits (ENOB)

- Spectral analysis using higher-frequency inputs used to characterize dynamic linearity (INL not defined)

- Invariably THD, SFDR, SNDR degrade with input frequency

- Effects of device noise due to random movement of electronics and parasitic device capacitances inherently the major factor limiting dynamic performance (clever design can drive non-noise undesired effects to arbitrarily low levels)

- Analytical modeling of dynamic linearity effects is challenging (nonlinear differential equations characterize the dynamic linearity effects)

DAC Architectures (Nyquist Rate)

Types

- Voltage Scaling
  - Resistor String DACs (string DACs)
  - Interpolating
- Current Steering
  - Binarily Weighted Resistors
  - R-2R Ladders
  - Current Source Steering
    - Thermometer Coded
    - Binary Weighted
    - Segmented
- Charge Redistribution
  - Switched Capacitor
- Serial
  - Algorithmic
  - Cyclic or Re-circulating
  - Pipelined
- Integrating
- Resistor Switching
- MDACs (multiplying DACs)

DAC Architectures

Structures

- Hybrid or Segmented
- Mode of Operation
  - Current Mode
  - Voltage Mode
  - Charge Mode
- Self-Calibrating
  - Analog Calibration
    - Foreground
    - Background
  - Digital Calibration
    - Foreground
    - Background
  - Dynamic Element Matching
- Laser of Link Trimmed
- Thermometer Coded or Binary
- Radix 2 or non-radix 2
- Inherently Monotone

DAC Architectures

- Type of Classification may not be unique nor mutually exclusive
- Structure is not mutually exclusive
- All approaches listed are used (and probably some others as well)
- Some are much more popular than others
  - Popular Architectures
    - Resistor String (interpolating)
    - Current Source Steering (with segmentation)
- Many new architectures are possible and some may be much better than the best currently available
- All have perfect performance if parasitic and matching performance are ignored !
- Major challenge is in determining appropriate architecture and managing the parasitics

Nonideal Effects of Concern

- Matching
- Parasitic Capacitances
  (including Charge injection)
- Loading
- Nonlinearities
- Previous code dependence
- Code-dependent settling
- Interconnect resistors
- Noise
- Slow and plagued by jitter
- Temperature Effects
- Aging
- Package stress

Observations

- Yield Loss is the major penalty for not appropriately managing parasitics and matching and this loss can be ruthless
- The ultimate performance limit of essentially all DACs is the yield loss associated with parasitics and matching
- Many designers do not have or use good statistical models that accurately predict data converter performance
- If you work of a company that does not have good statistical device models
  - Convince model groups of the importantc of dedveloping these models
  - (or) develop appropriate test strutures to characterize your process
- Existing nonlinear device models may not sufficiently accurately predict device nonlinearities for high-end data converter applications

Observations

- Experienced Designers/Companies often produce superior data converter products
- Essentially all companies have access to the same literature, regularly reverse engineer successful competitors products and key benefits in successful competitors products are generally not locked up in patents
- High-end designs(speed and resolution) may get attention in the peer community but practical moderate performance converters usually make the cash flow
- Area (from a silicon cost viewpoint) is usually not the driving factor in high-end designs where attractive price/mfg cost ratios prevail

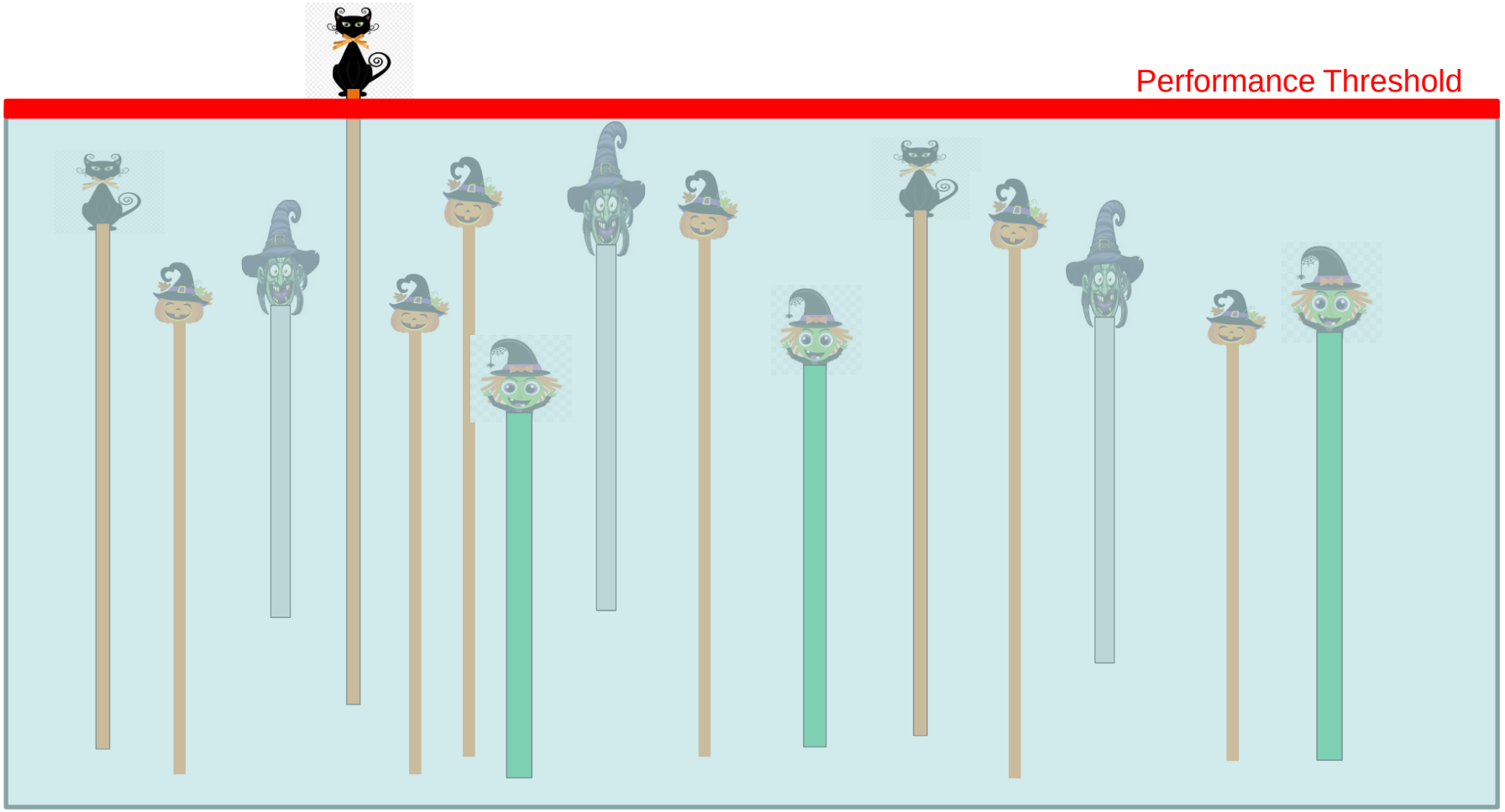
Data Converter Design Strategies

- There are many different DAC and ADC architectures that have been proposed and that are in widespread use today
- Almost all work perfectly if all components are ideal
- Most data converter design work involves identifying the contributors to nonideal performance and finding work-arounds to these problems
- Some architectures are more difficult to find work-arounds than others
- All contributors to nonidealities that are problematic at a given resolution of speed level must be identified and mitigated
- The nonidealities generally fall into one of two categories
  - Matching-critical nonidealities (degrade yield)
  - Component nonidealities (degrade performance even if desired matching is present)

Data Converter Design Strategies

Remember:

Need to keep nonideal effects below an acceptable performance threshold



Identifying Problems/Challenges and Clever/Viable Solutions

- Many problems occur repeatedly so should recognize when they occur
- Identify clever solutions to basic problems – they often are useful in many applications
- Don't make the same mistake twice !

The problem:

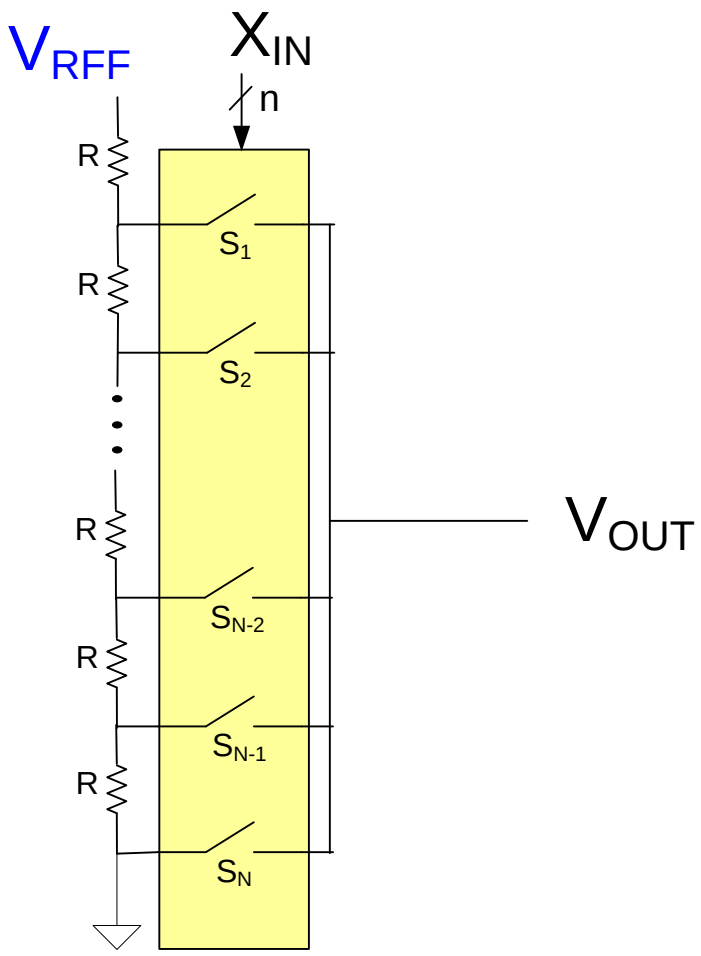
The perceived solution:

The practical or clever solution:

The List !

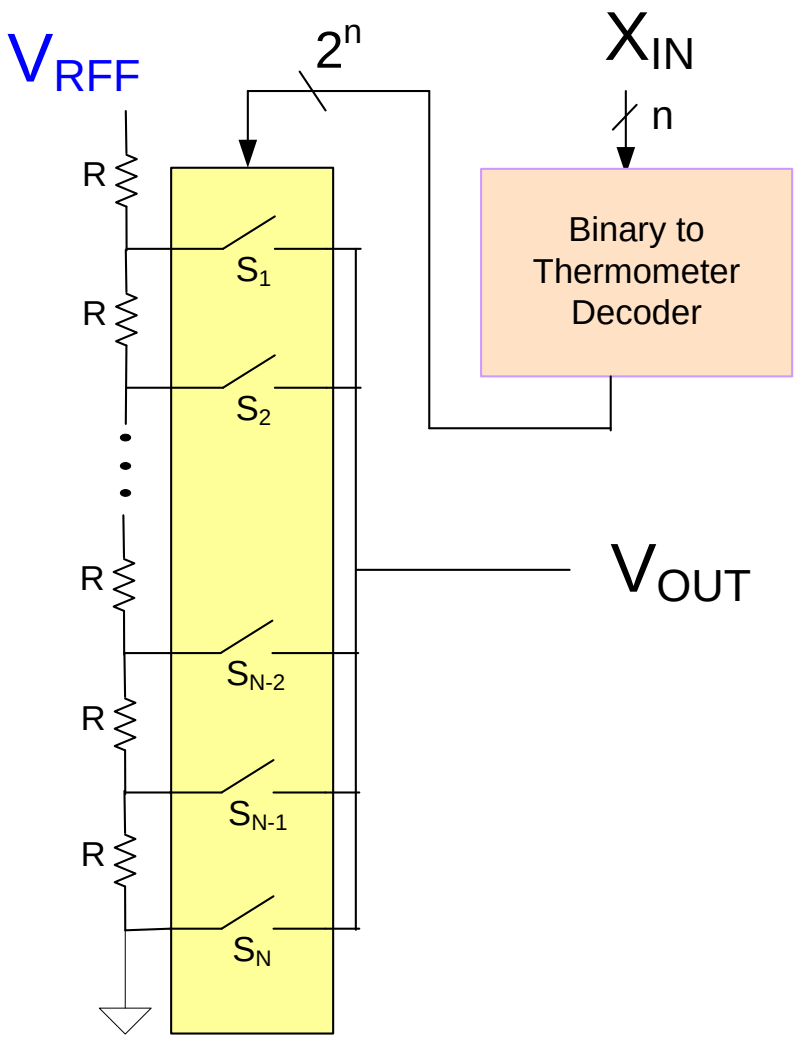
The List Keeper !

R-String DAC



Basic R-String DAC

R-String DAC



Basic R-String DAC including Logic to Control Switches

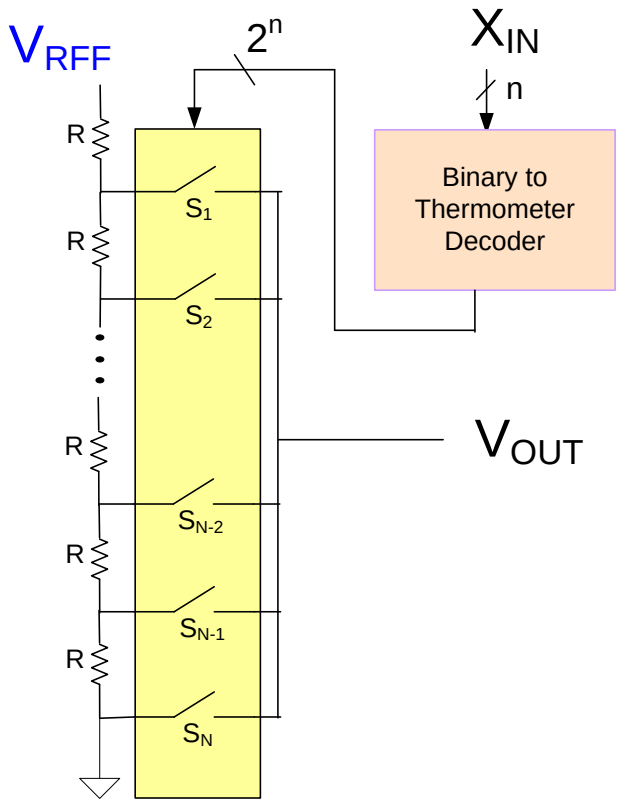
R-String DAC

If all components are ideal, performance of the R-string DAC is that of an ideal DAC!

Key Properties of R-String DAC

- One of the simplest DAC architectures
- R-string DAC is inherently monotone

Possible Limitations or Challenges



R-String DAC

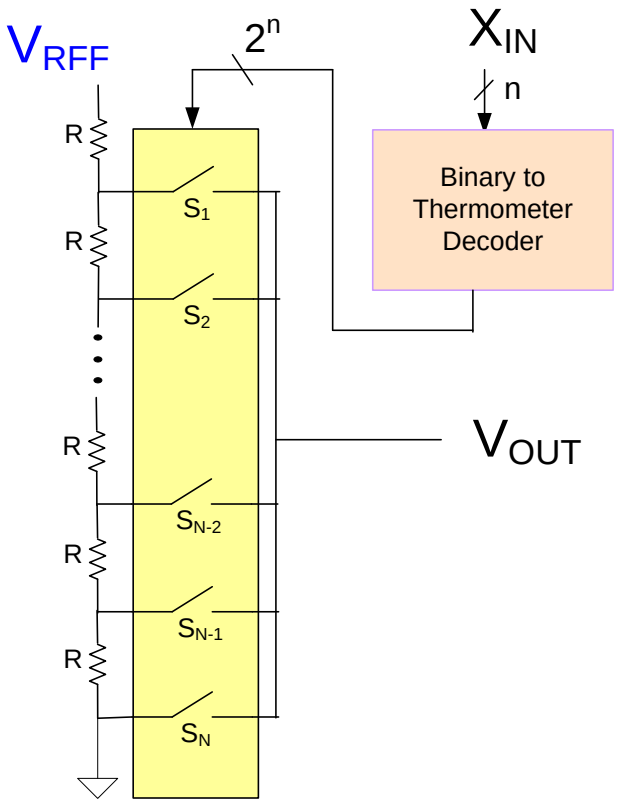
If all components are ideal, performance of the R-string DAC is that of an ideal DAC!

Key Properties of R-String DAC

- One of the simplest DAC architectures
- R-string DAC is inherently monotone

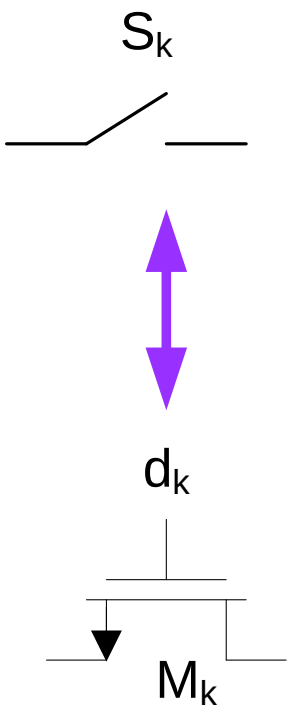
Possible Limitations or Challenges

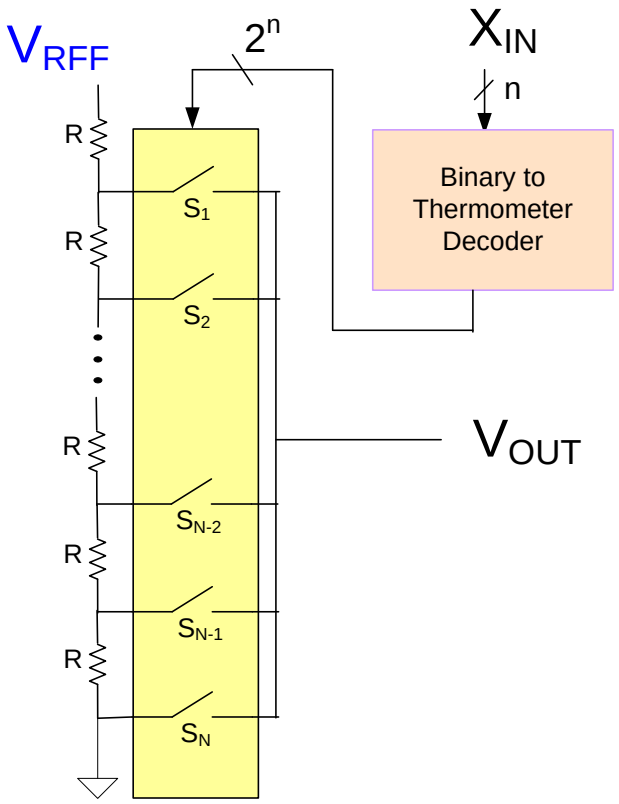
- Binary to Thermometer Decoder (BTTD) gets large for n large
- Logic delays in BTTD may degrade performance
- Matching of the resistors may not be perfect
  - Local random variations
  - Gradient effects
- How can switches be made ?
- Lots of capacitance on output node



R-String DAC

Typical strategy for implementing the switch



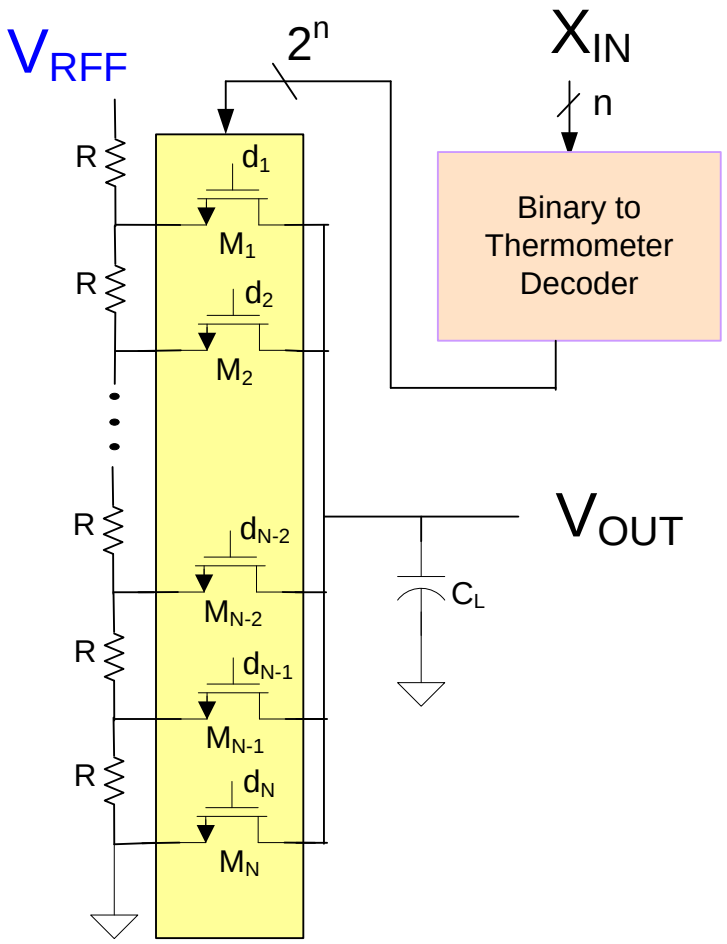


- **Switch array is an analog MUX**
- **Very simple structure**
- **Switch array combined with the BTTD forms a 2^n:1 analog MUX**

R-String DAC

R-String DAC with MOS switches

Possible Limitations:



R-String DAC

R-String DAC with MOS switches

Possible Limitations:

Switch impedance is not 0

Switch may not even turn on at all if V_{REF} is large

Switch impedance is input-code dependent

Time constants are input-code dependent

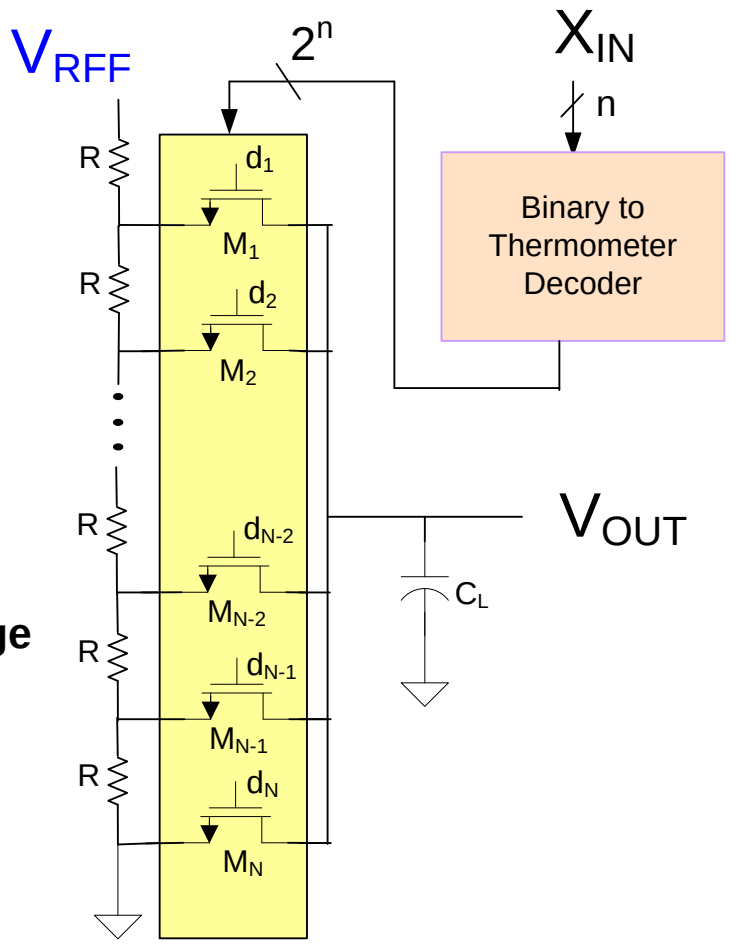
Transition times are previous-code dependent

C_L has 2^n diffusion capacitances so can get very large
(will discuss this issue next)

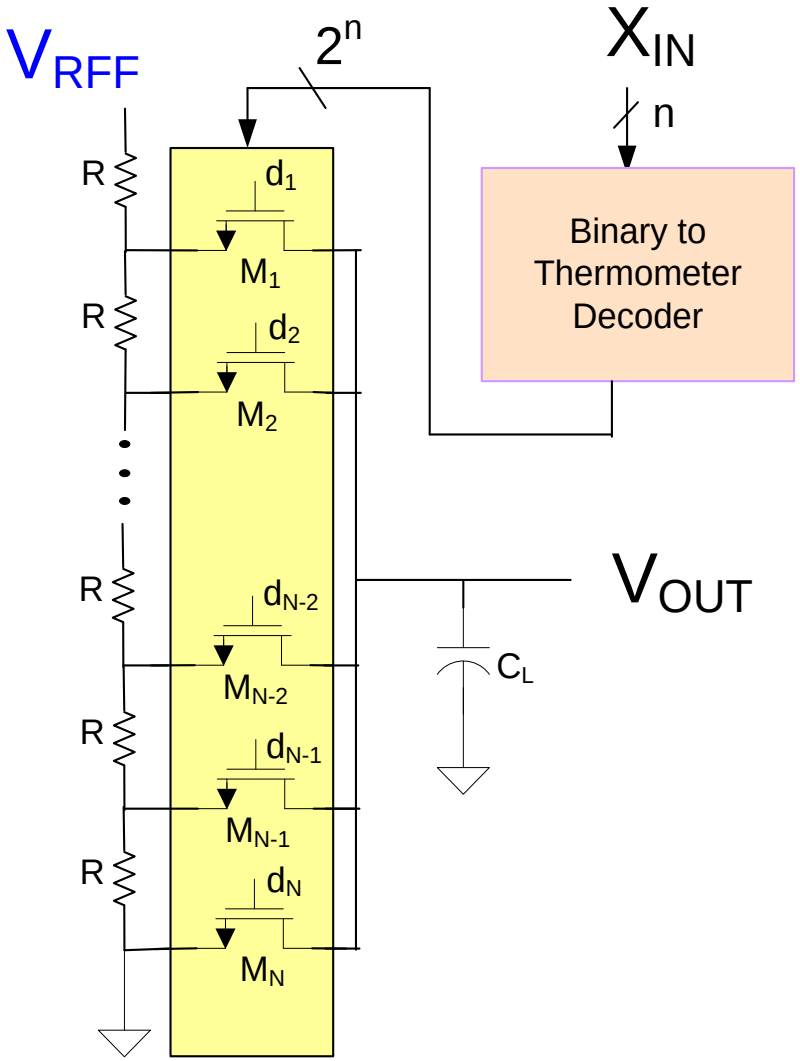
Mismatch of resistors
- **local random variation**
- **gradient effects**

Decoder can get very large for n large

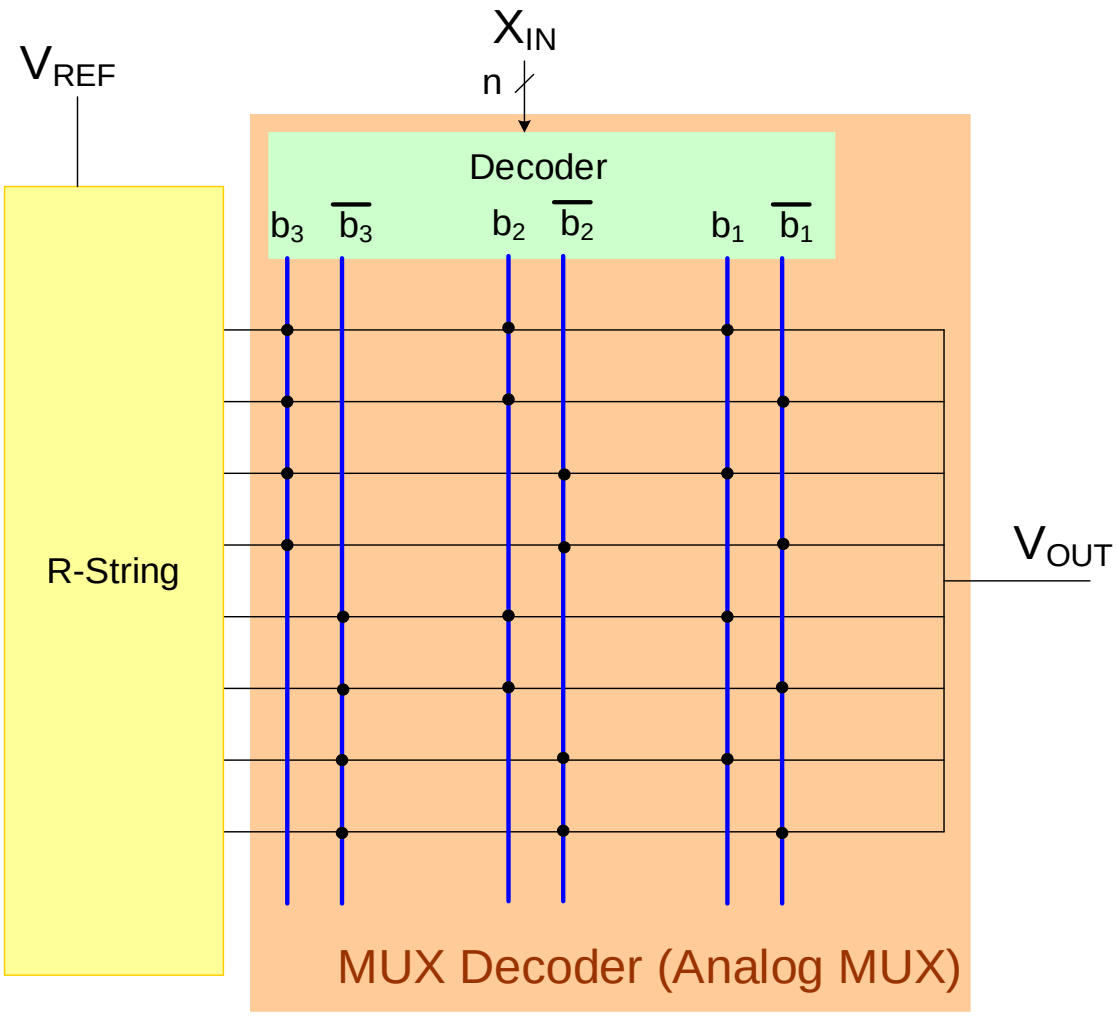
Routing of the 2^n switch signals can become very long and consume lots of area



Basic R-String DAC



R-String DAC



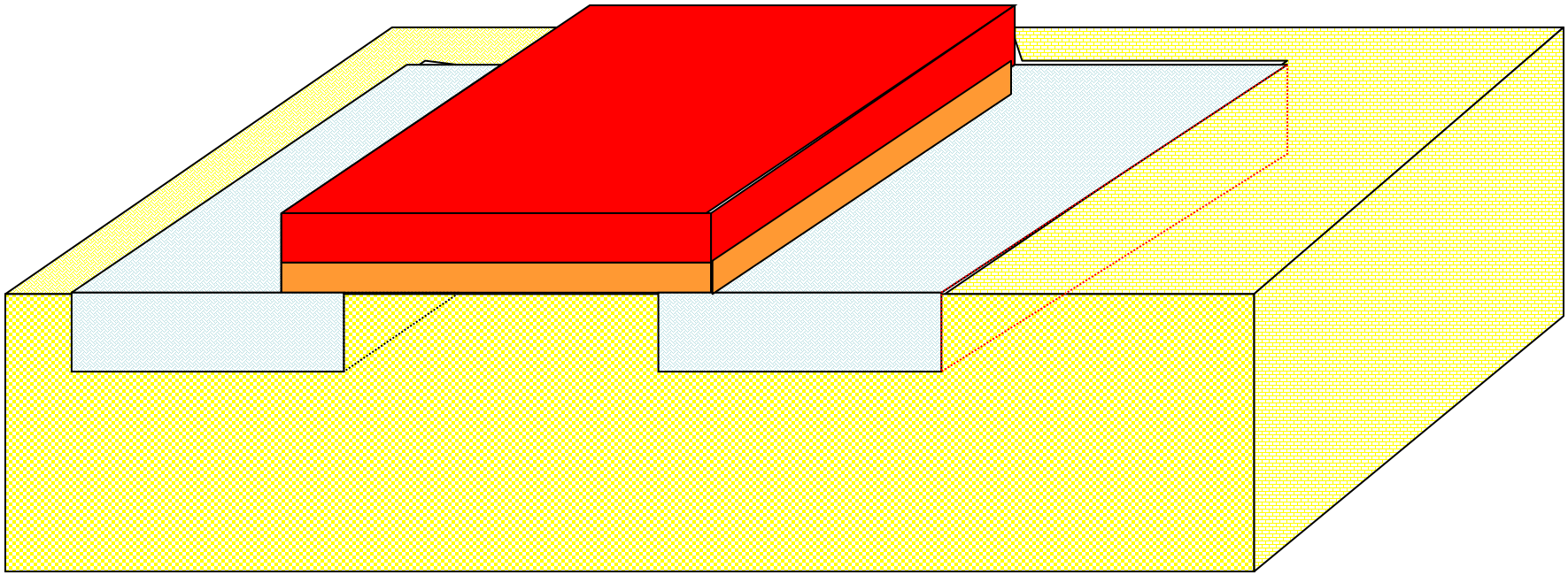
MUX decoder is comprised of analog AND gates

Logic Synthesis not used to form MUX

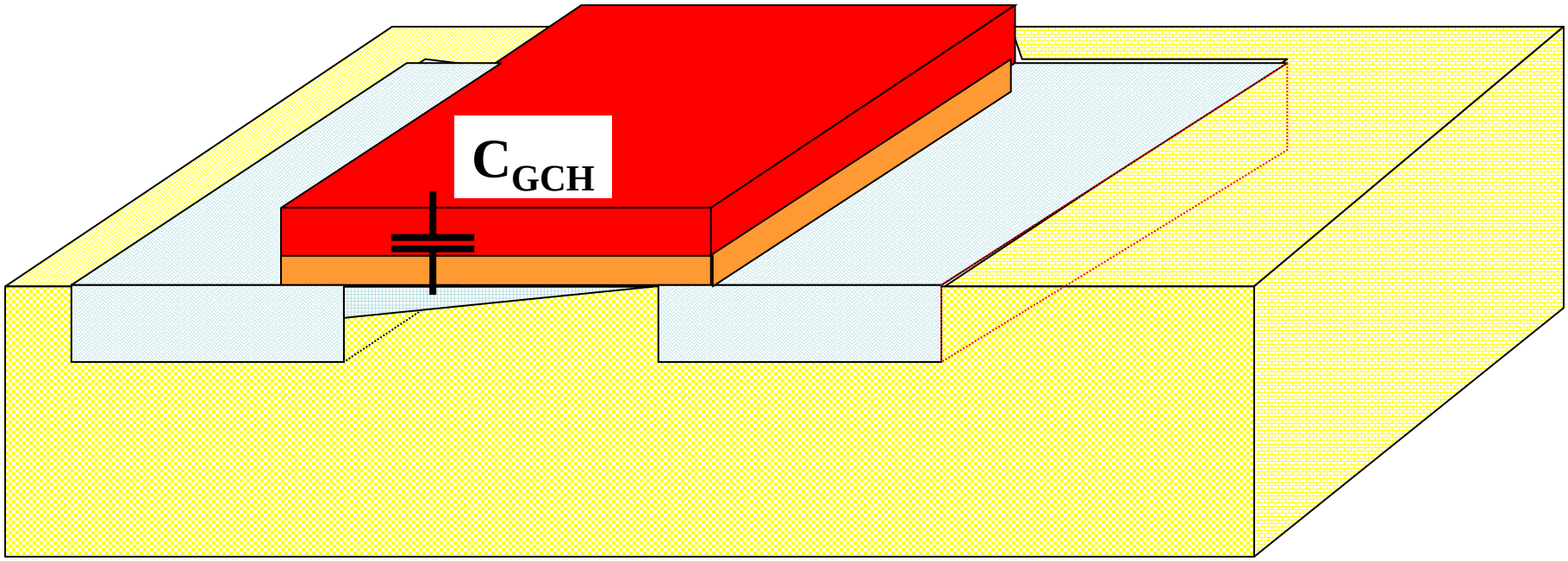
(Review from: EE 330)

Parasitic Capacitors in MOSFET

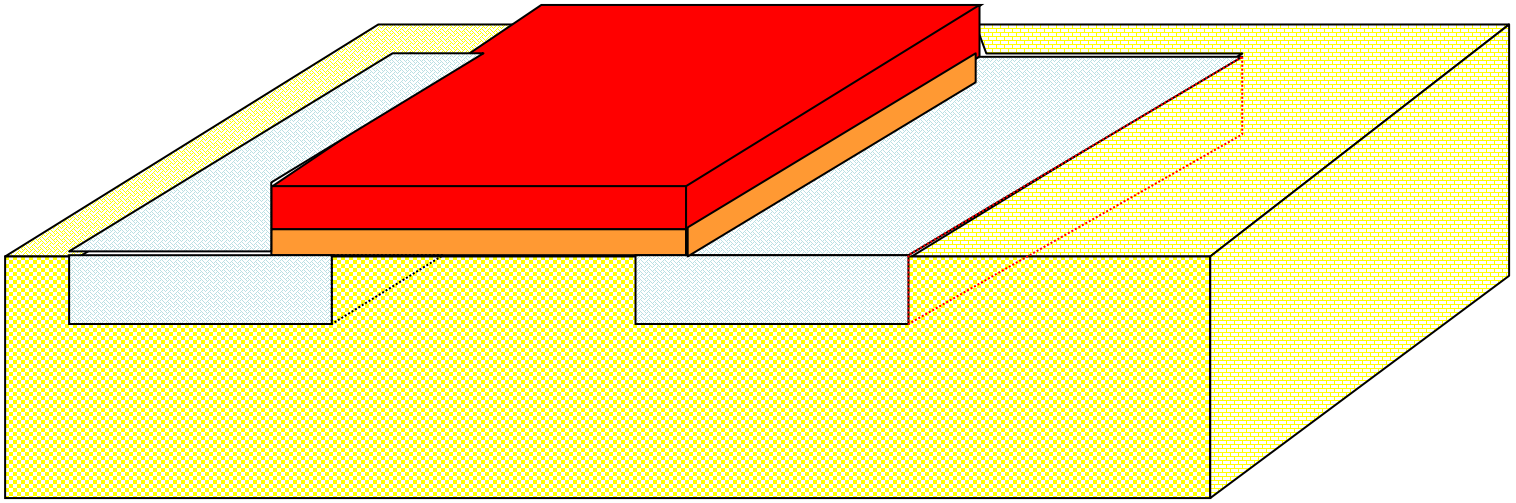
(initially assume saturation and consider two: Gate-channel and diffusion)



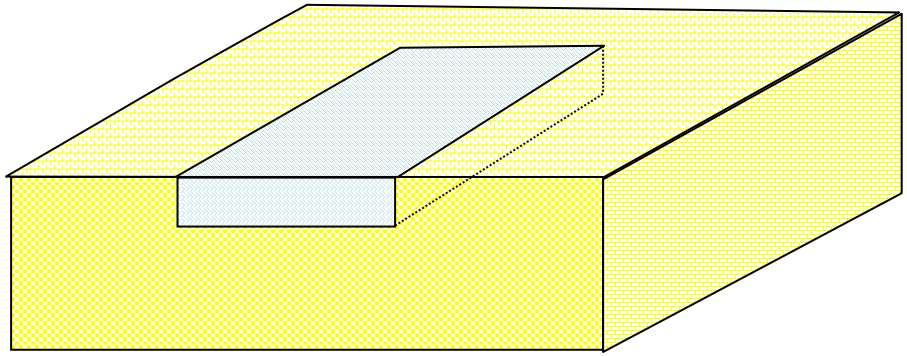
Parasitic Capacitors in MOSFET



Parasitic Capacitors in MOSFET

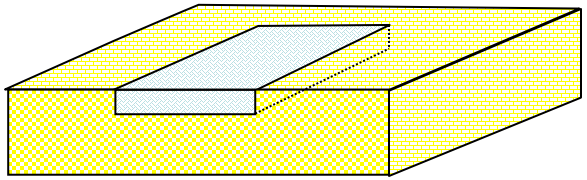


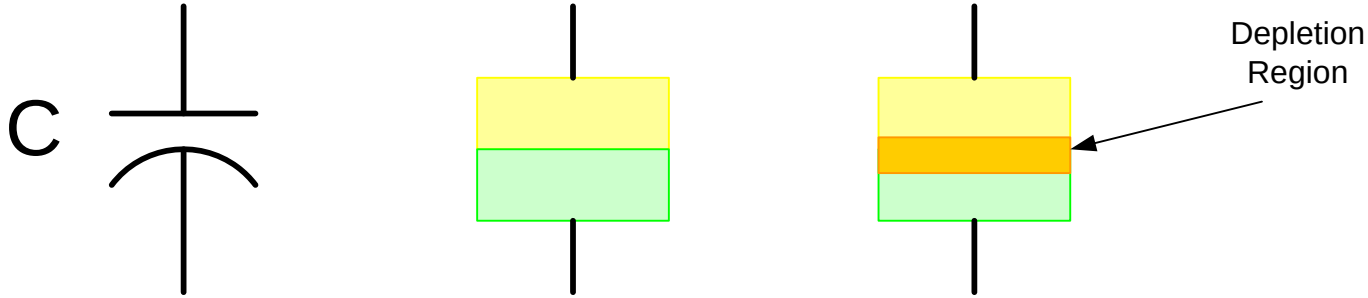
Recall that pn junctions have a depletion region!



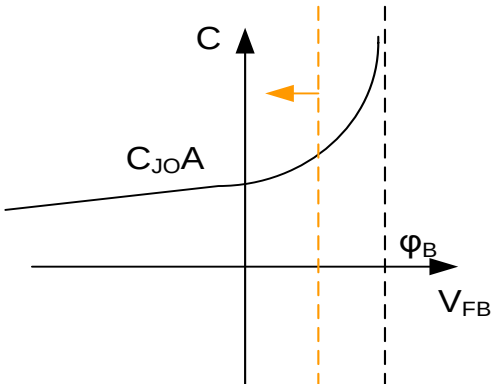
Parasitic Capacitors in MOSFET

pn junction capacitance





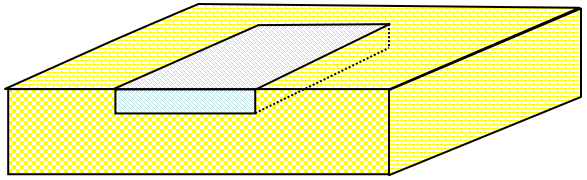
For $V_{FB}<\varphi_B/2$



$$C = \frac{C_{J0} A}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

Parasitic Capacitors in MOSFET

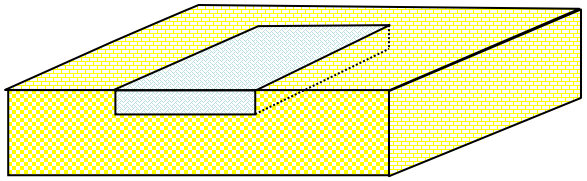
pn junction capacitance

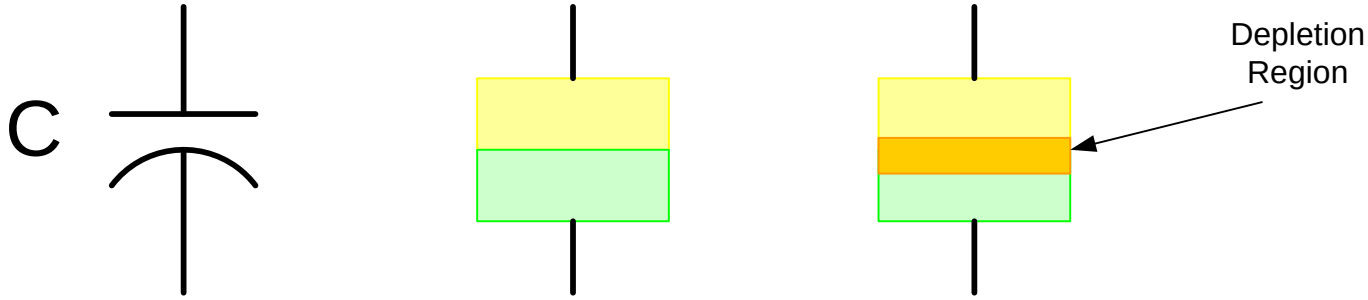


The bottom and the sidewall:

Parasitic Capacitors in MOSFET

pn junction capacitance





For a pn junction capacitor

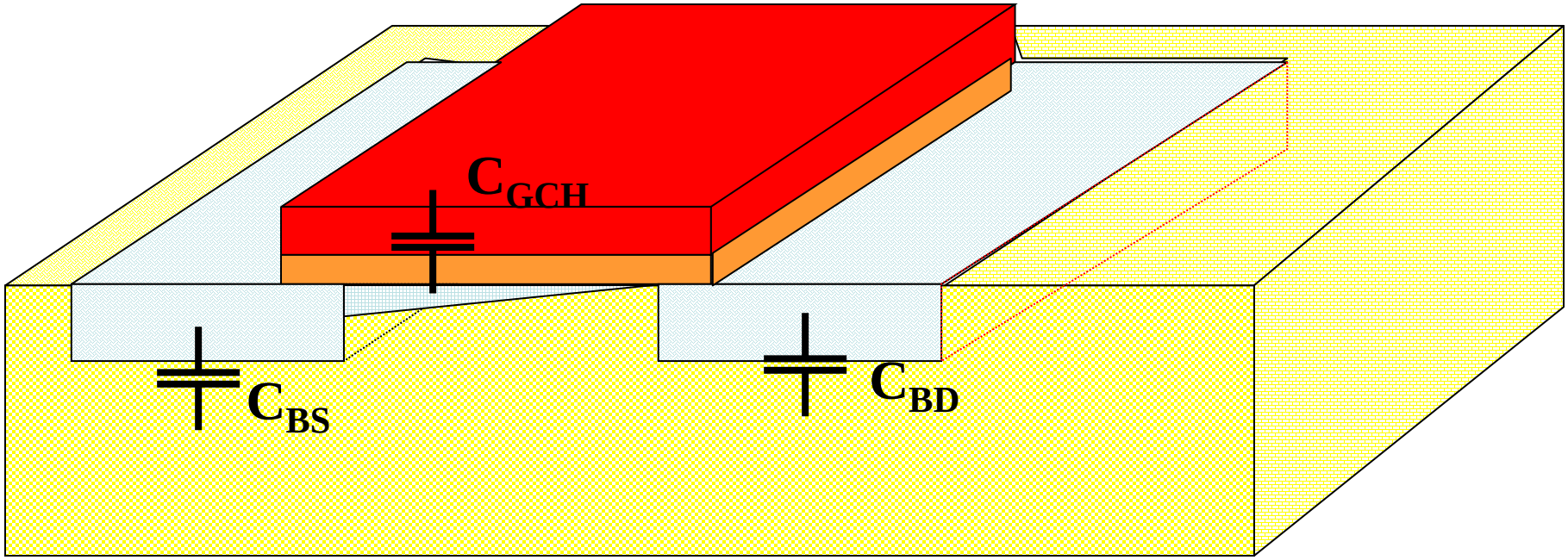
$$C_J = C_{BOT} A + C_{SW} P$$

$$C_{BOT} = \frac{C_{BOT} A}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

$$C_{SW} = \frac{C_{SW} P}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

Parasitic Capacitors in MOSFET

(initially assume saturation and consider two: Gate-channel and diffusion)



- Diffusion capacitances nonlinear (dependent upon voltage)
- Many more actually present
- Operating region may affect parasitics

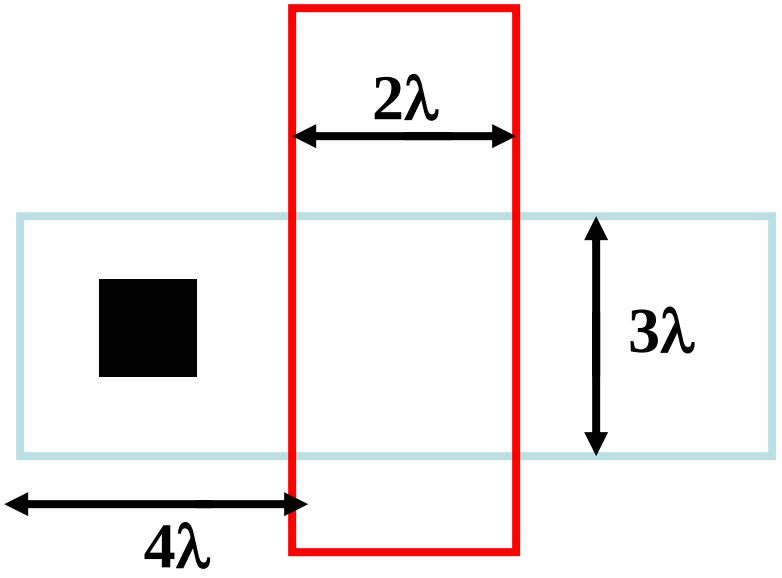
Question

- Are the parasitic capacitors relevant?

Observation

- Parasitic Capacitors are Small

Consider a minimum-sized transistor



Process Parameters from ON 0.5u Process

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_	HR POLY2	MTL1	MTL2	UNITS
Sheet Resistance	81.5	101.9	21.6	1120	41	0.09	0.09	ohms/sq
Contact Resistance	64.6	141.9	15.8		26.8		0.8	ohms
Gate Oxide Thickness	140							angstrom

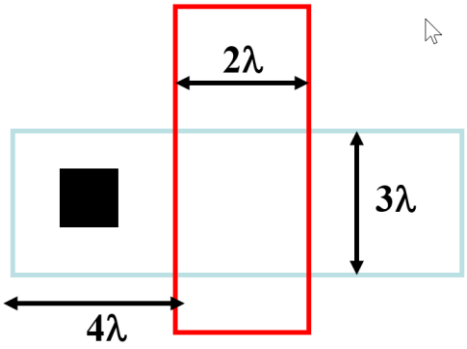
PROCESS PARAMETERS	MTL 3	N\PLY	N WELL					
Sheet Resistance	0.06	822	812					ohms/sq
Contact Resistance	0.65							ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	424	731	87		32	16	10	39	aF/um^2
Area (N+active)			2473		36	16	12		aF/um^2
Area (P+active)			2382						aF/um^2
Area (poly)				969	56	15	10		aF/um^2
Area (poly2)					50				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							39		aF/um^2
Fringe (substrate)	315	247			72	58	38		aF/um
Fringe (poly)					57	39	28		aF/um
Fringe (metal1)						48	34		aF/um
Fringe (metal2)							55		aF/um
Overlap (N+active)			195						aF/um
Overlap (P+active)			239						aF/um

λ=0.3 microns

Size of Capacitances



Gate-Channel Capacitance = $6\lambda^2$ x 2.47fF/μ^2 = 1.33fF

Source Diffusion-Substrate Capacitance =
$12\lambda^2$ x .424fF/μ^2 + 14λ x .315fF/μ =
.46fF + 1.32fF =1.78fF

Note Sidewall Capacitance larger than Bottom Capacitance

Are these negligible?

Are these negligible?

These small capacitors play the dominant role in the speed limitations of most digital circuits

These small capacitors play a major role in the performance of many linear circuits

It is essential that these capacitors (parasitic capacitors) be considered and managed when designing most integrated circuits today!

Types of Capacitors

1. Fixed Capacitors
   a. Fixed Geometry
   b. Junction

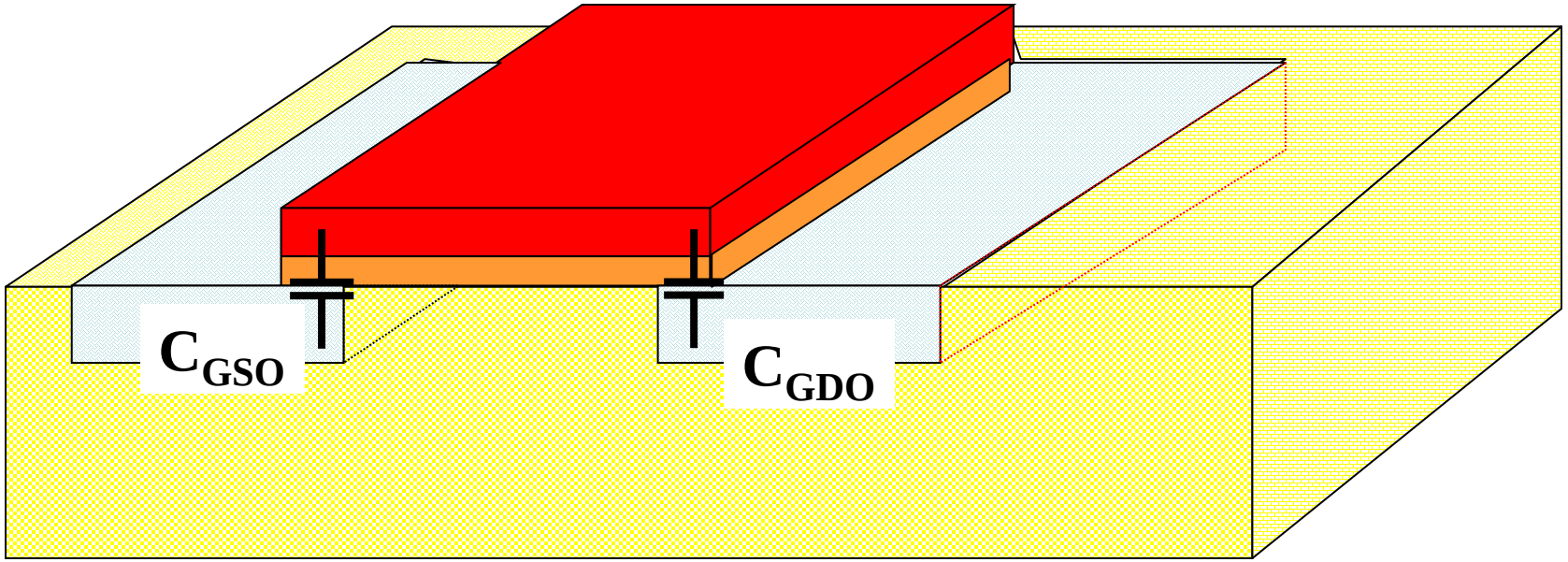
2. Operating Region Dependent
   a. Fixed Geometry
   b. Junction

Parasitic Capacitors in MOSFET

Fixed Capacitors

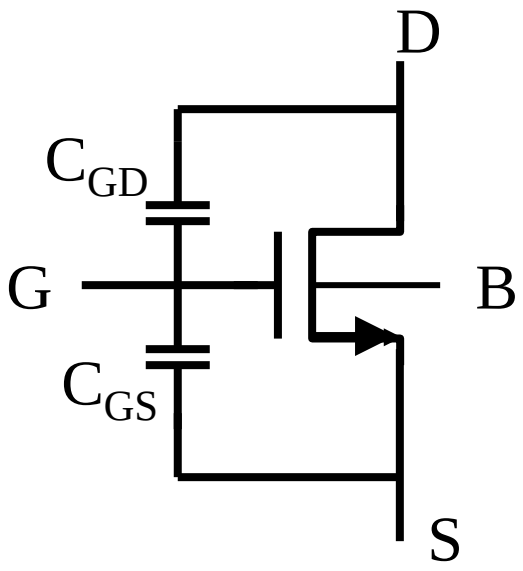
Parasitic Capacitors in MOSFET

Fixed Capacitors



Overlap Capacitors: C_{GDO}, C_{GSO}

Fixed Parasitic Capacitance Summary

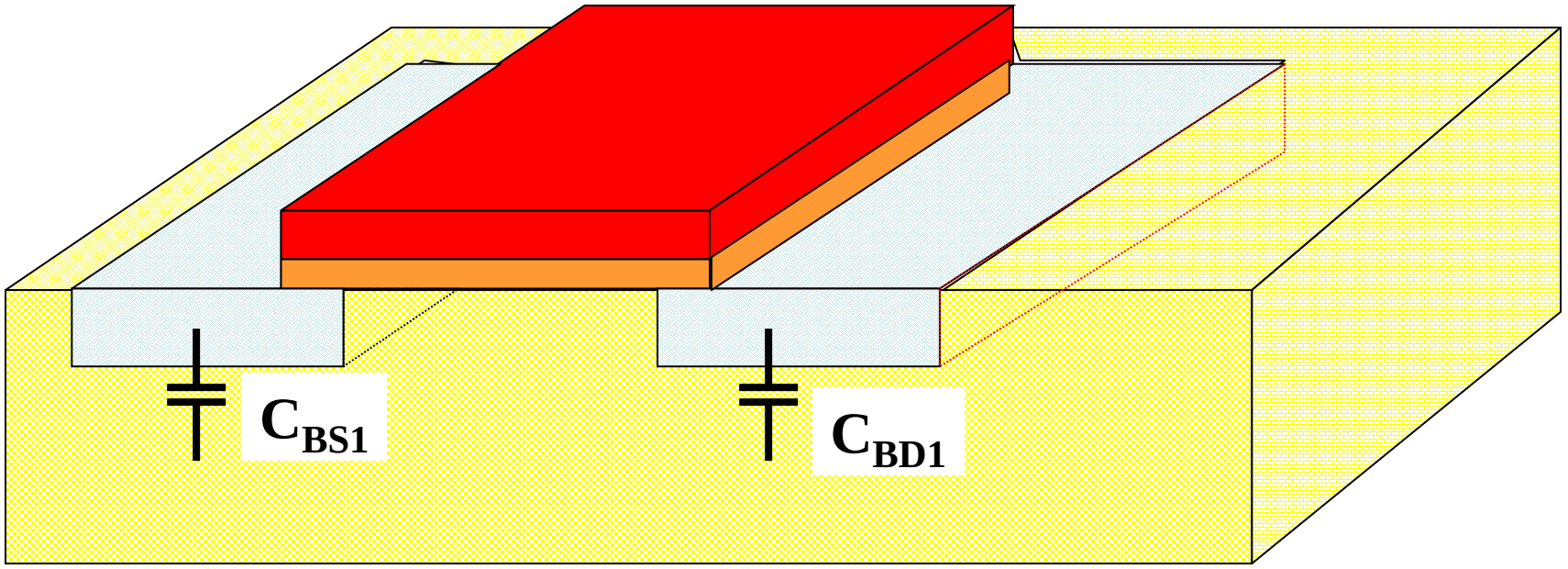


	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{GD}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$

L_D is a model parameter

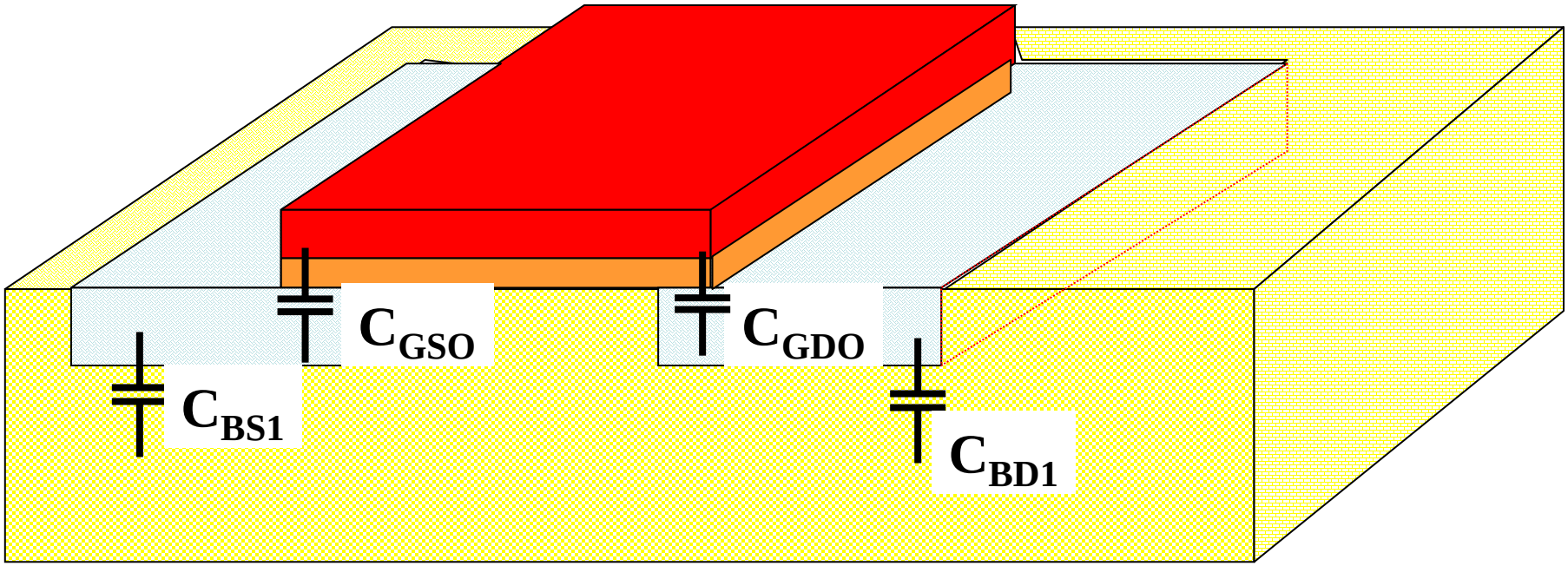
Parasitic Capacitors in MOSFET

Fixed Capacitors



Junction Capacitors: C_{BS1}, C_{BD1}

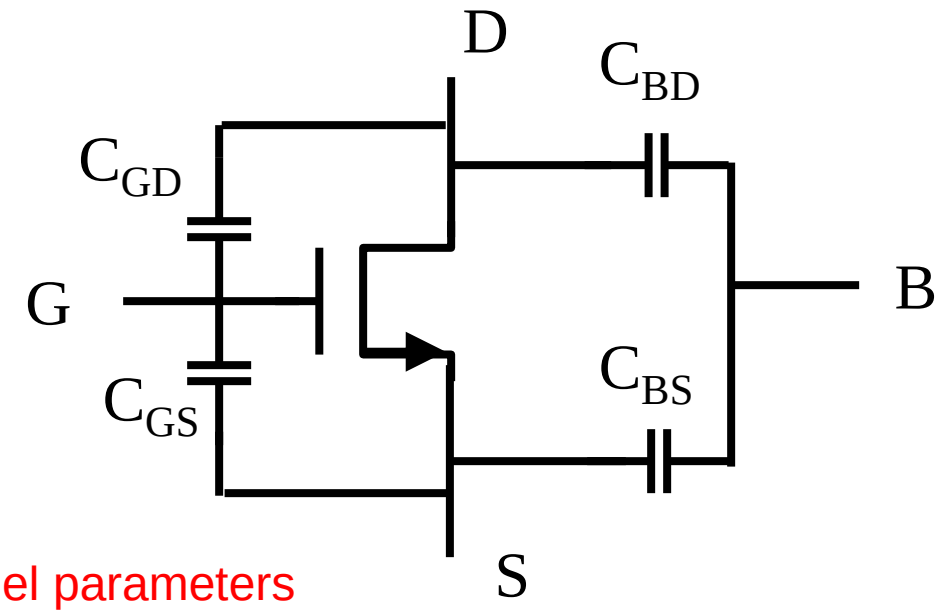
Parasitic Capacitors in MOSFET
Fixed Capacitors



Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Fixed Parasitic Capacitance Summary



C_{BOT} and C_{SW} are model parameters

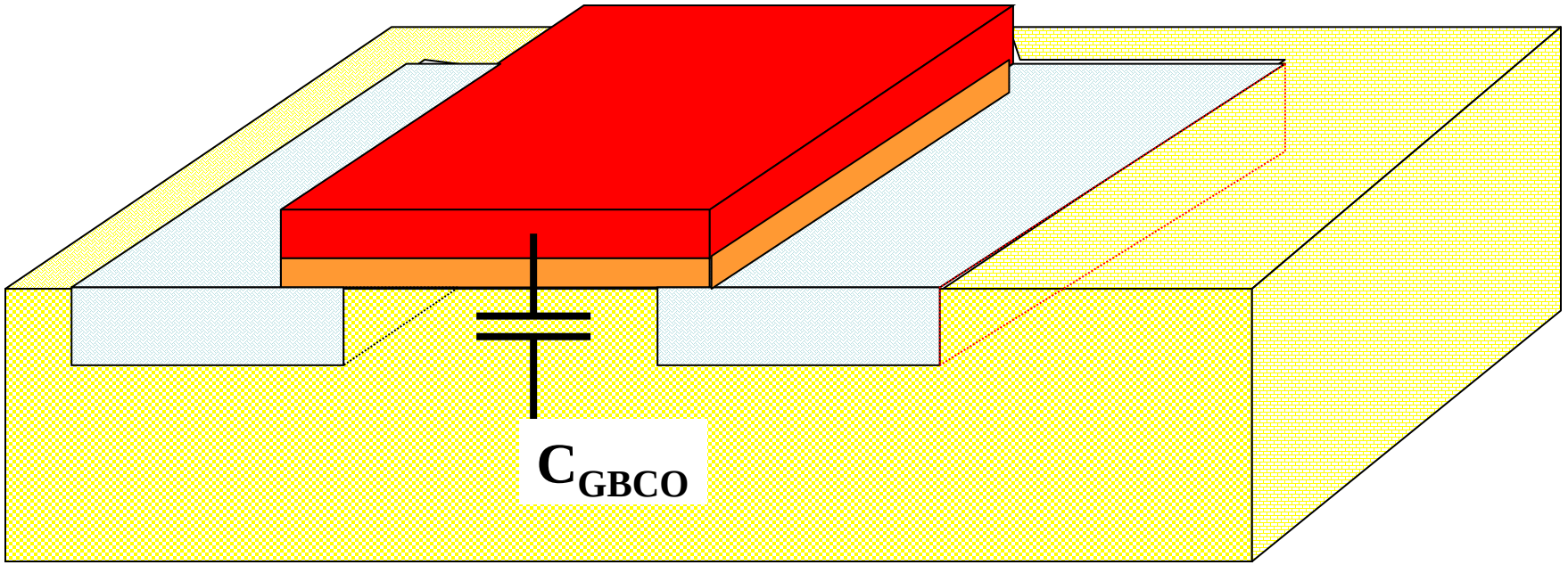
	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{GD}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{BG}			
C_{BS}	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$
C_{BD}	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$

Parasitic Capacitors in MOSFET

Operation Region Dependent

Parasitic Capacitors in MOSFET

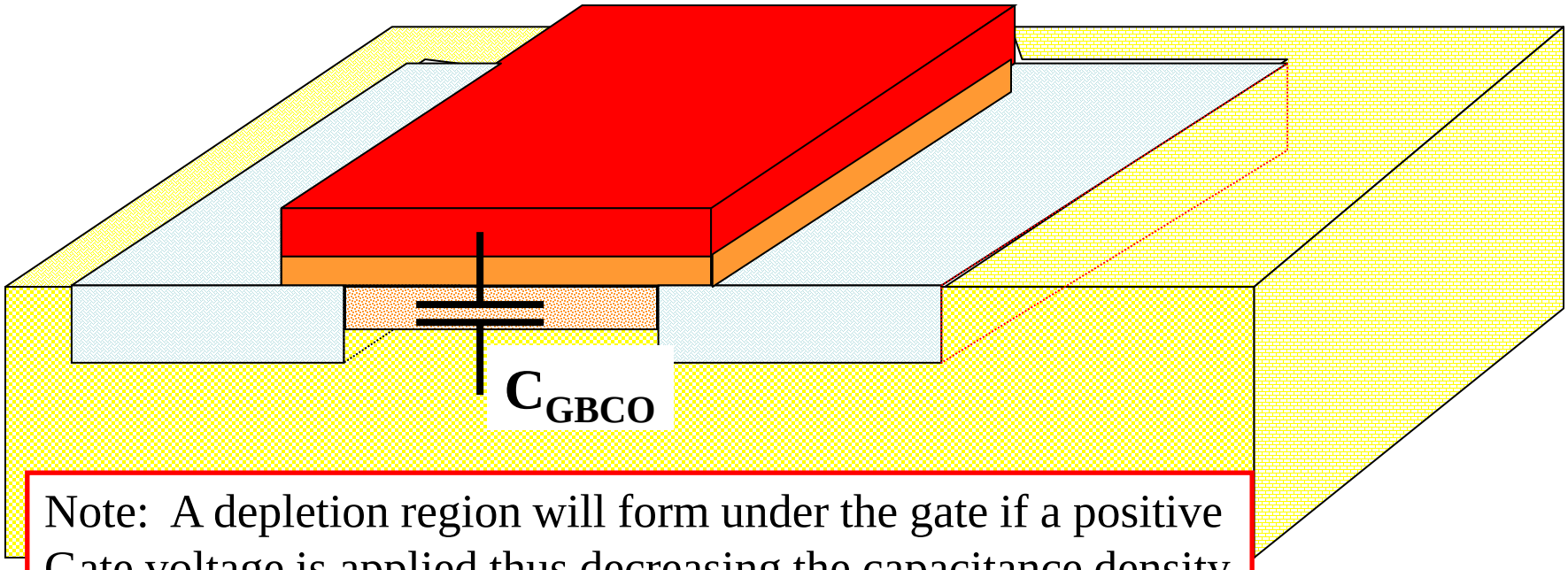
Operation Region Dependent -- Cutoff



Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Cutoff

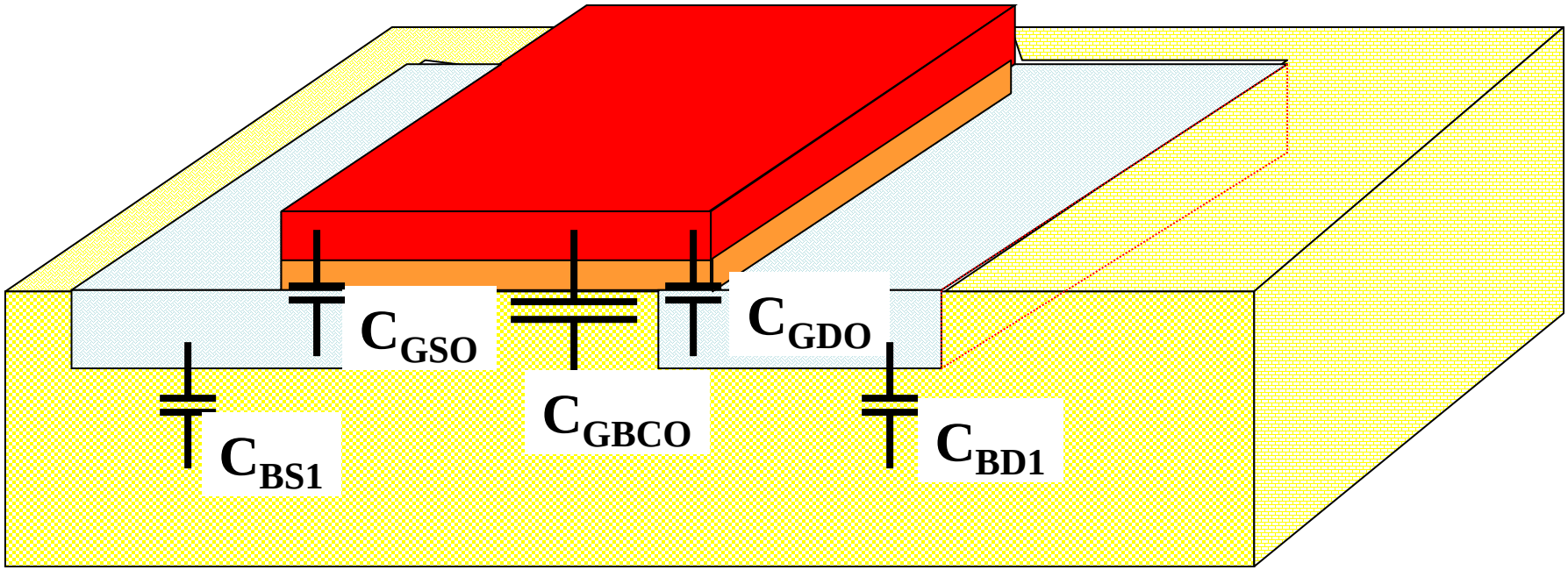


Note: A depletion region will form under the gate if a positive Gate voltage is applied thus decreasing the capacitance density

Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Cutoff

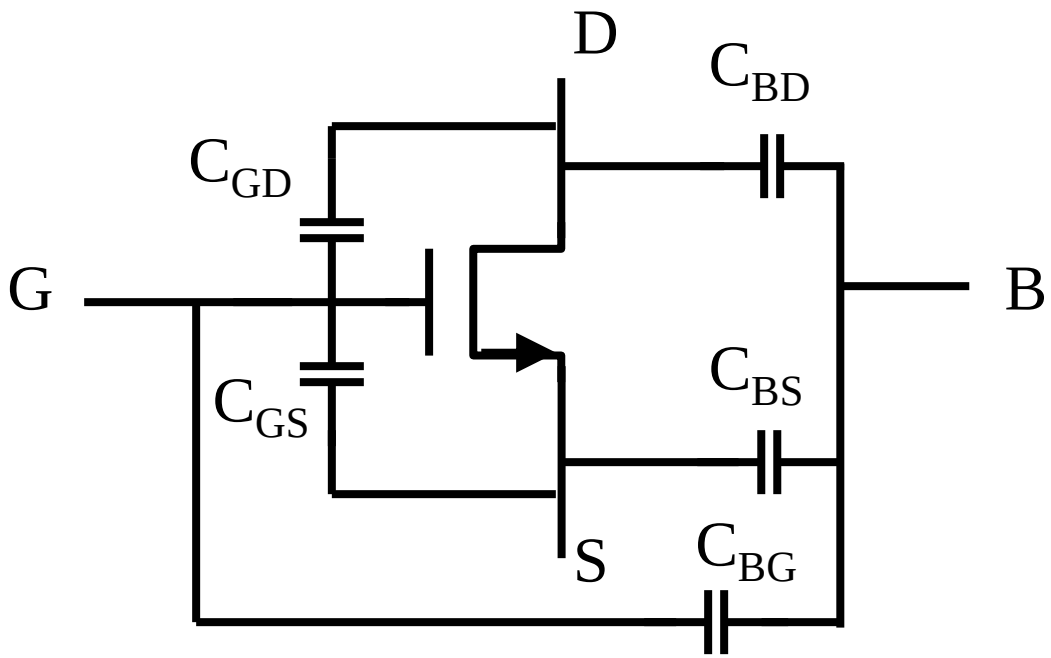


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Cutoff Capacitor: C_{GBCO}

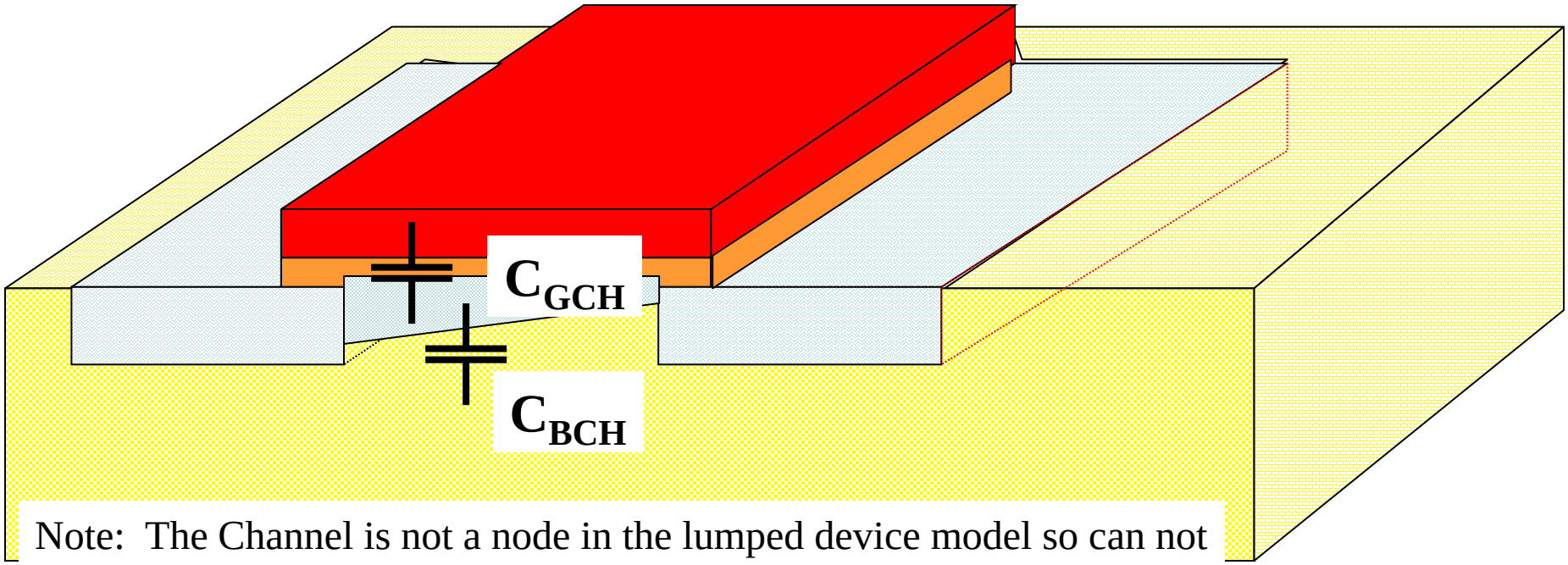
Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$		
C_{GD}	$CoxWL_D$		
C_{BG}	CoxWL (or less)		
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$		
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$		

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Ohmic



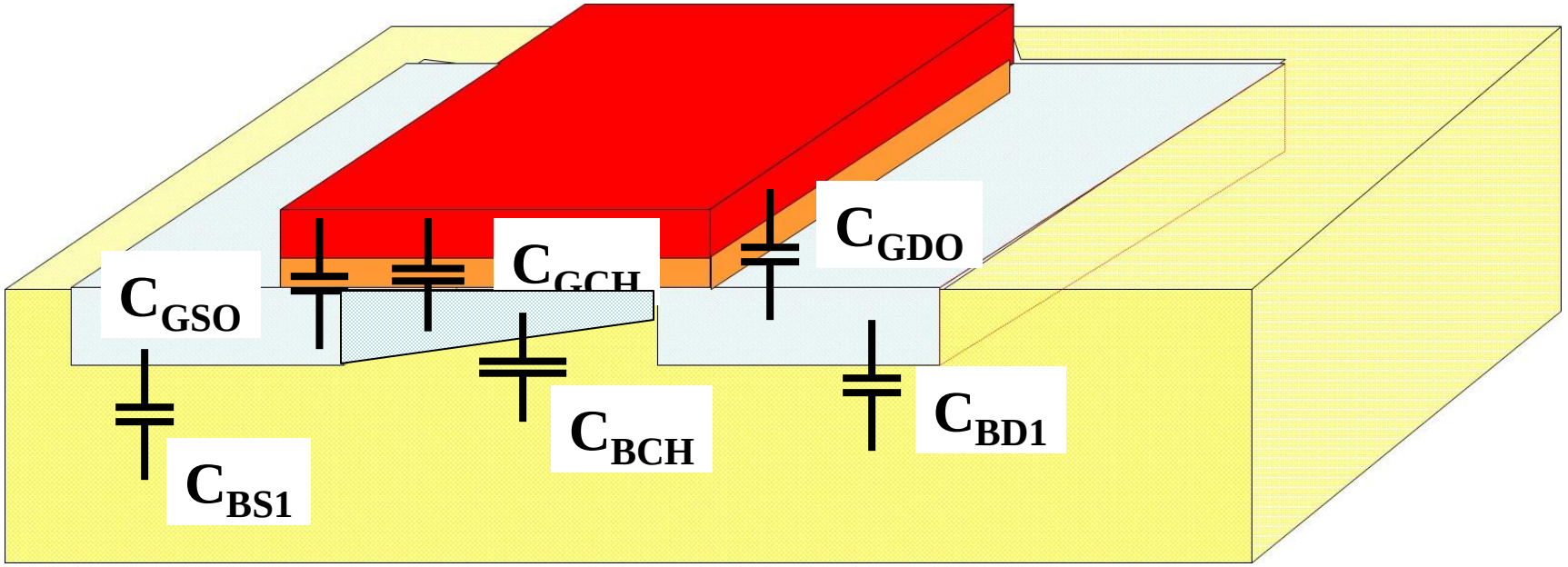
Note: The Channel is not a node in the lumped device model so can not directly include this distributed capacitance in existing models

Note: The distributed channel capacitance is usually lumped and split evenly between the source and drain nodes

Ohmic Capacitor: C_{GCH}, C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Ohmic

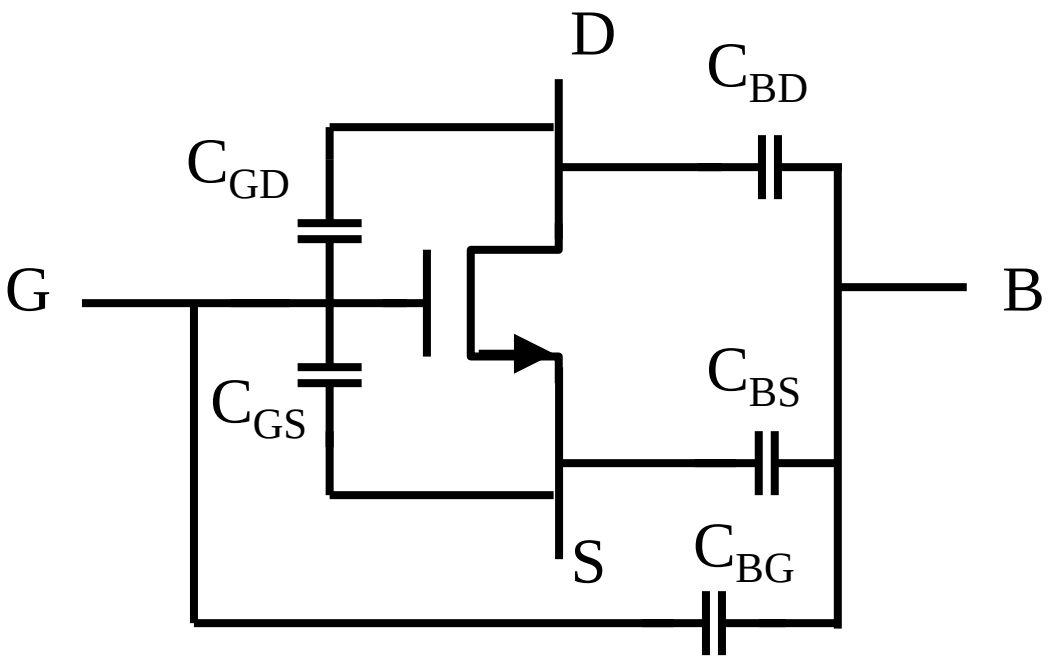


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Ohmic Capacitor: C_{GCH}, C_{BCH}

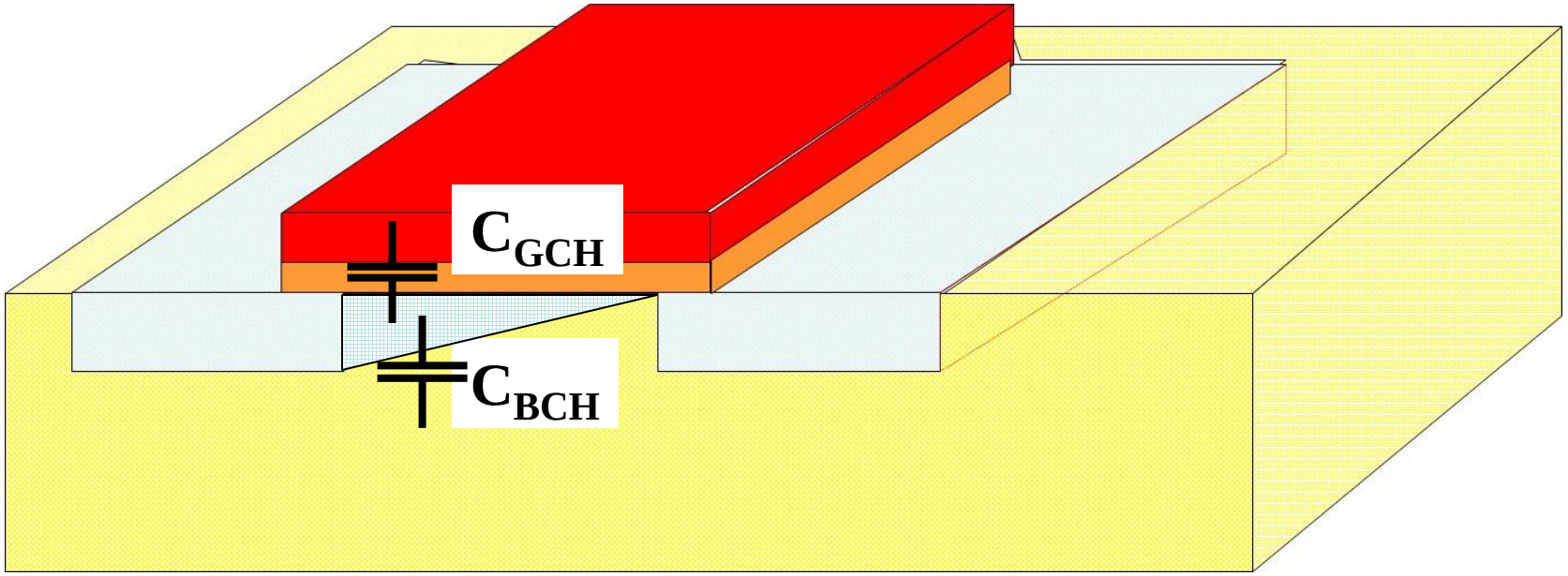
Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D$	
C_{GD}	$CoxWL_D$	$CoxWL_D$	
C_{BG}	CoxWL (or less)		
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Saturation

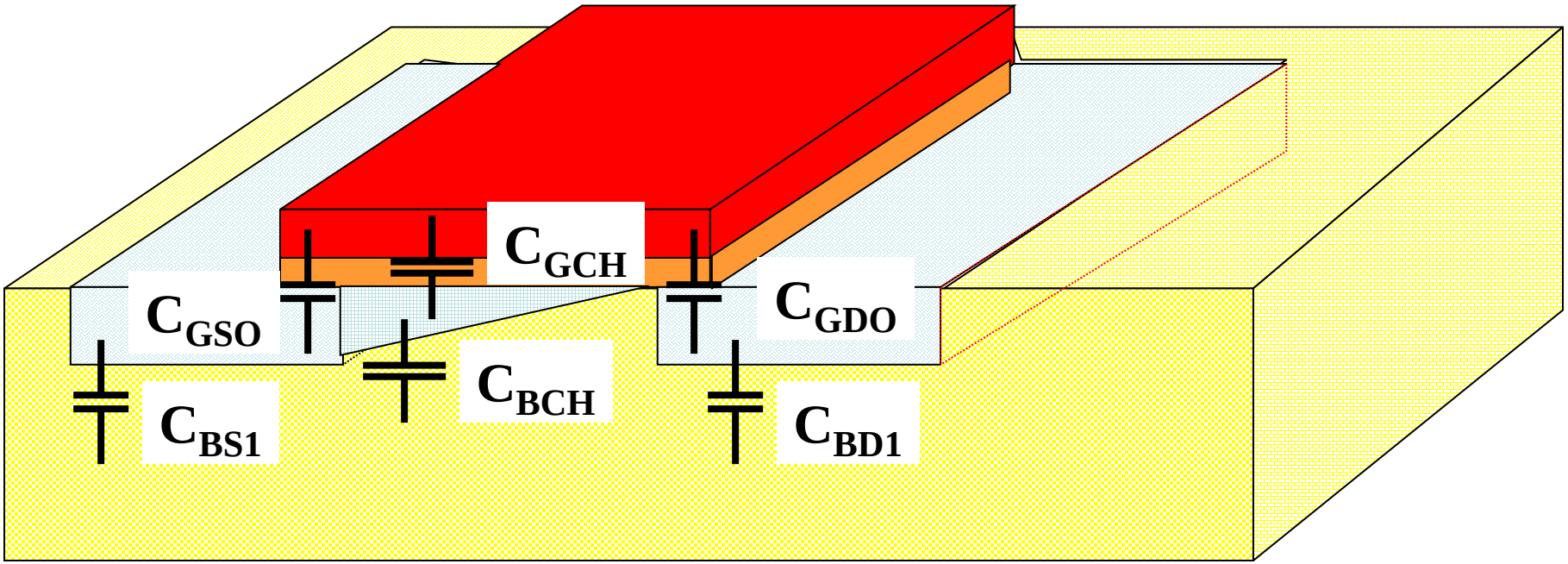


Note: Since the channel is an extension of the source when in saturation, the distributed capacitors to the channel are generally lumped to the source node

Saturation Capacitors: C_{GCH}, C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed --Saturation

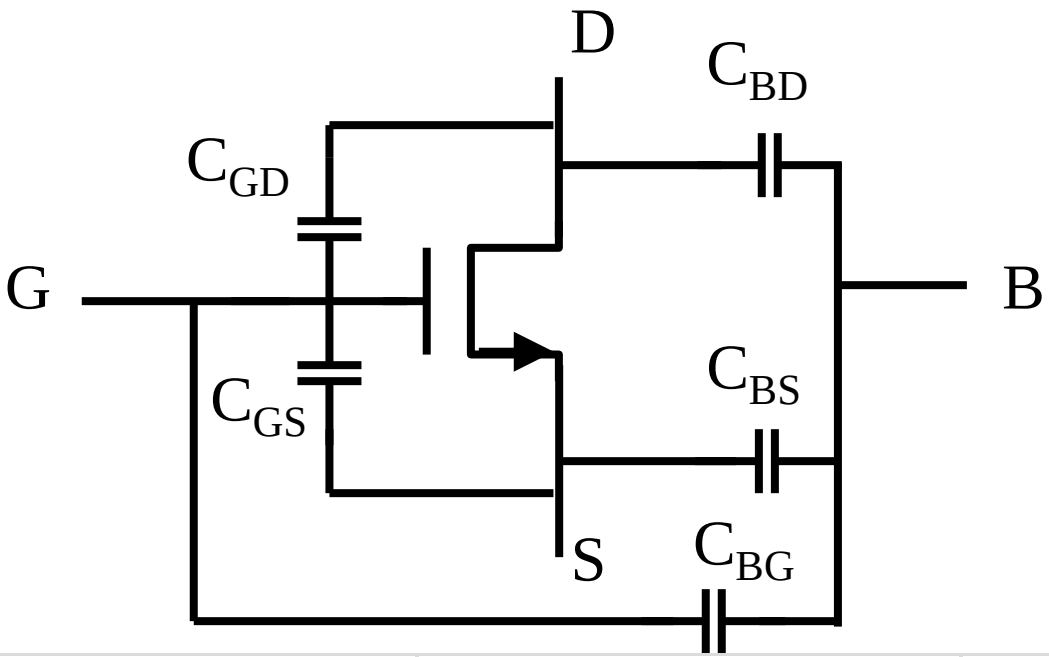


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

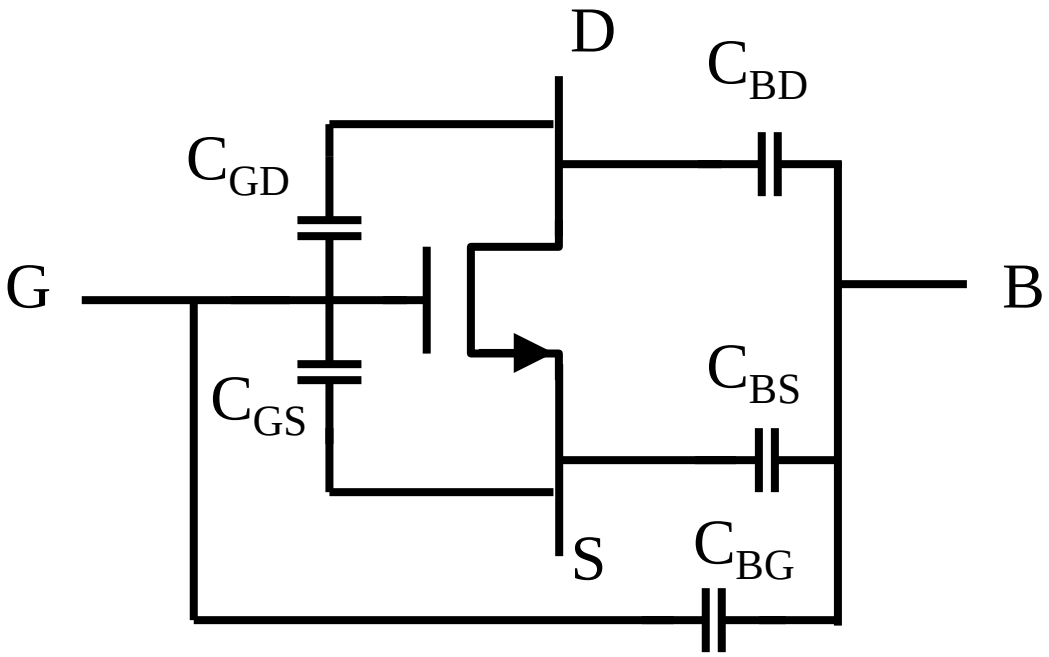
Saturation Capacitors: C_{GCH} , C_{BCH}

Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D+(2/3)C_{OX}WL$
C_{GD}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D$
C_{BG}	CoxWL (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S+(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

Parasitic Capacitance Summary

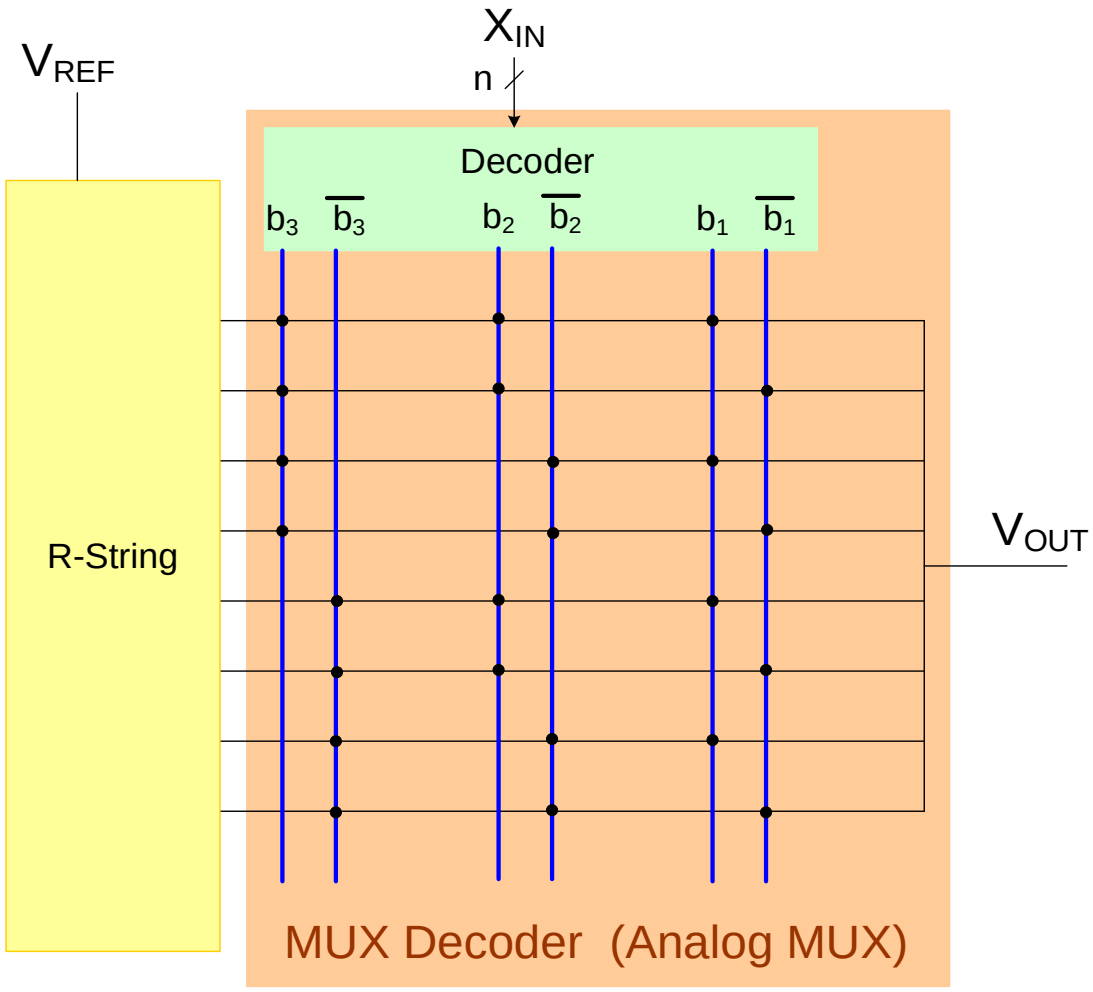


	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D+(2/3)C_{OX}WL$
C_{GD}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D$
C_{BG}	CoxWL (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S +(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

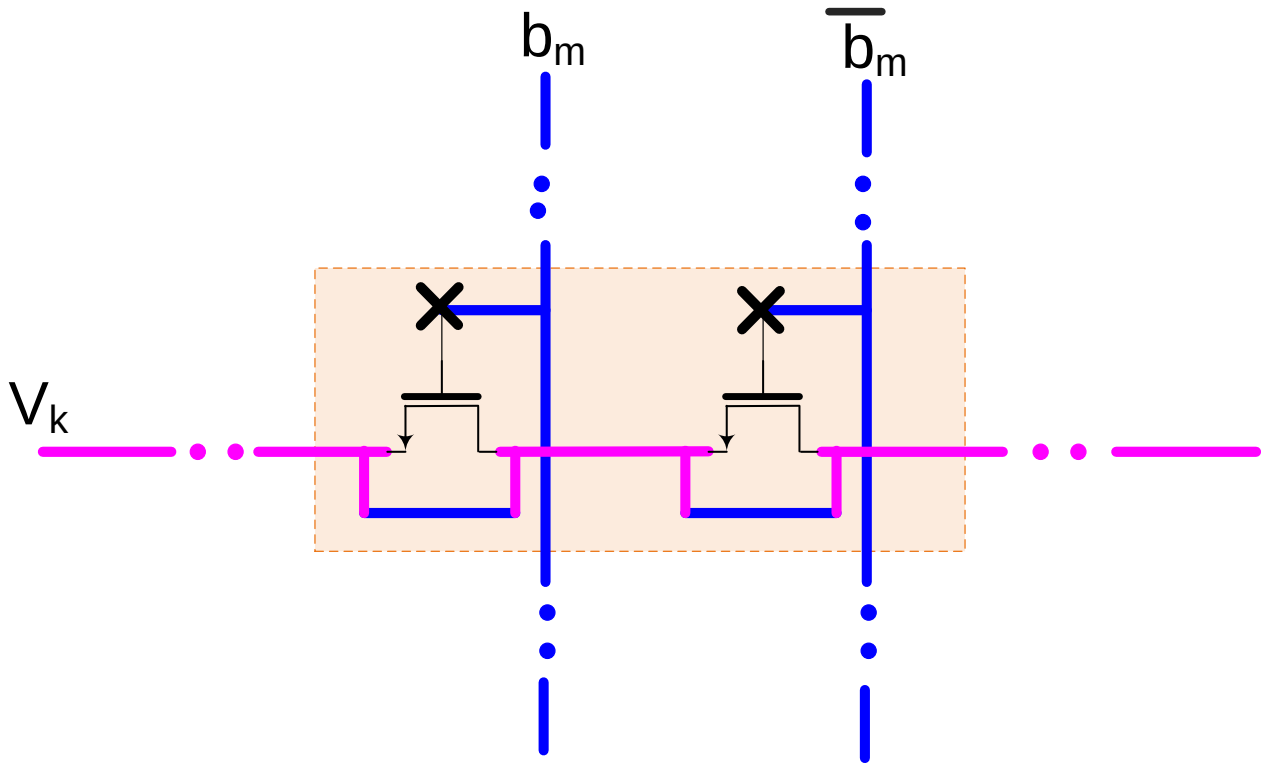
R-String DAC

MUX-Decoder Layout/Architecture

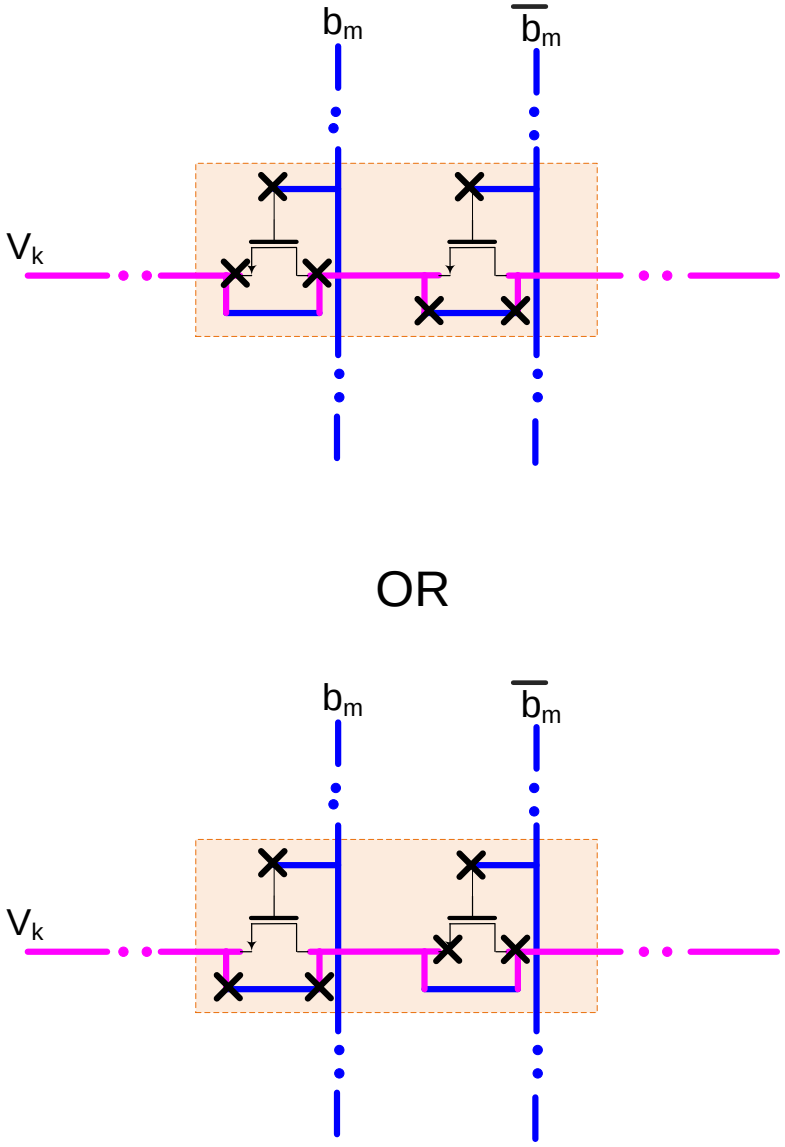
Each intersection is a reserved site for a switch



Uncontacted Row-Column Structure

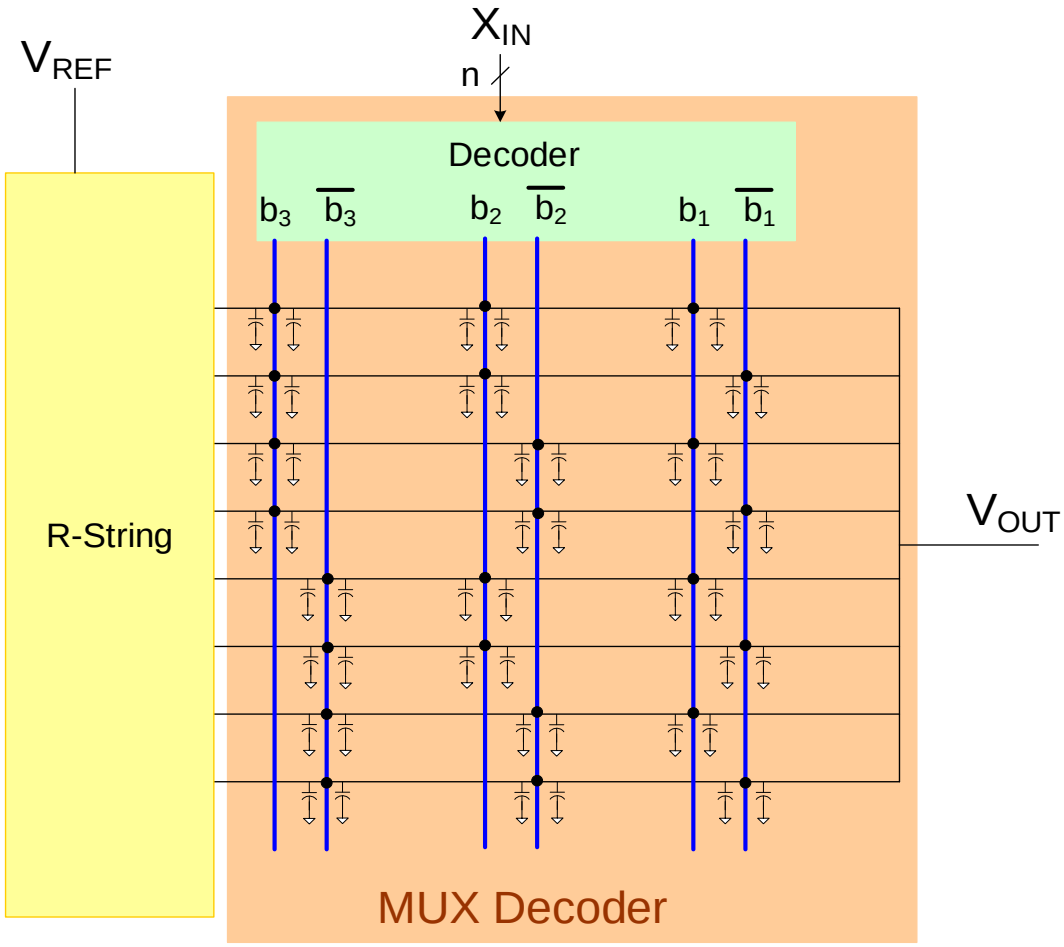


Row-Column Structure with Contacts Added



Programmed entirely with the contact mask

R-String DAC

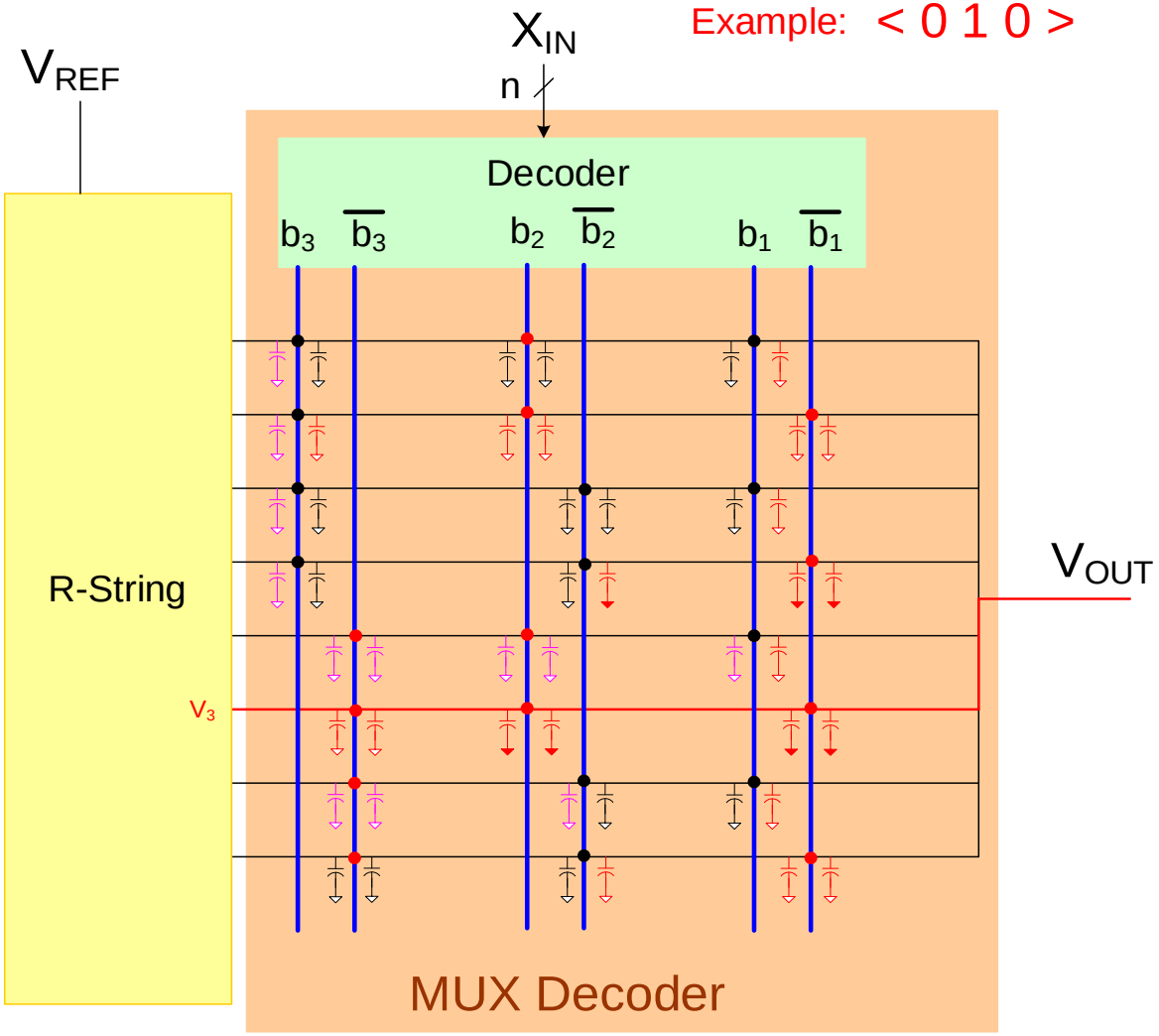


Parasitic Capacitances in MUX Decoder

(for convenience have not shown non-contacted transistor effects)

Previous code-dependent settling introduces distortion !

R-String DAC



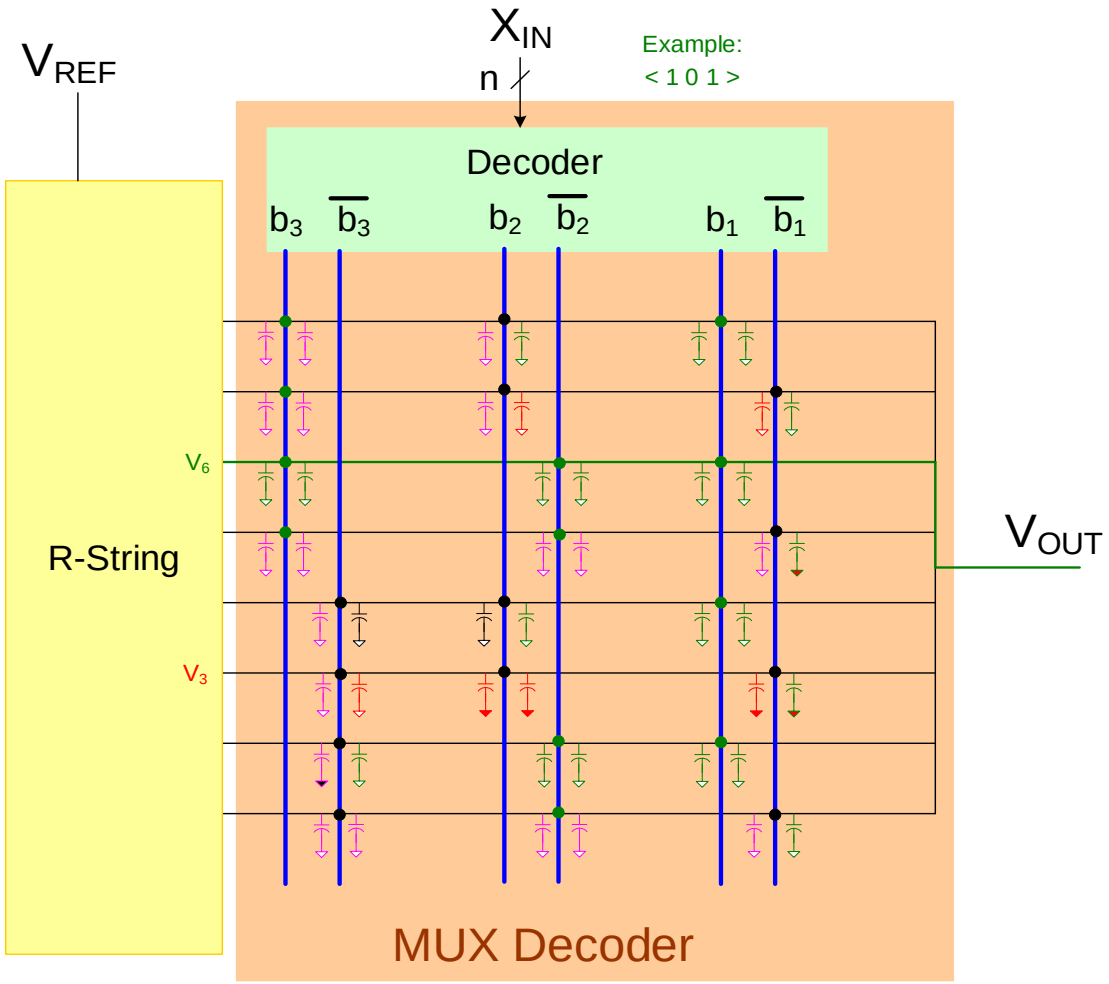
Previous-Code Dependent Settling

Assume all C's initially with 0V

Red denotes V_3, black denotes 0V, Purple some other voltage

R-String DAC

Transition from <010> to <101>



Previous-Code Dependent Settling

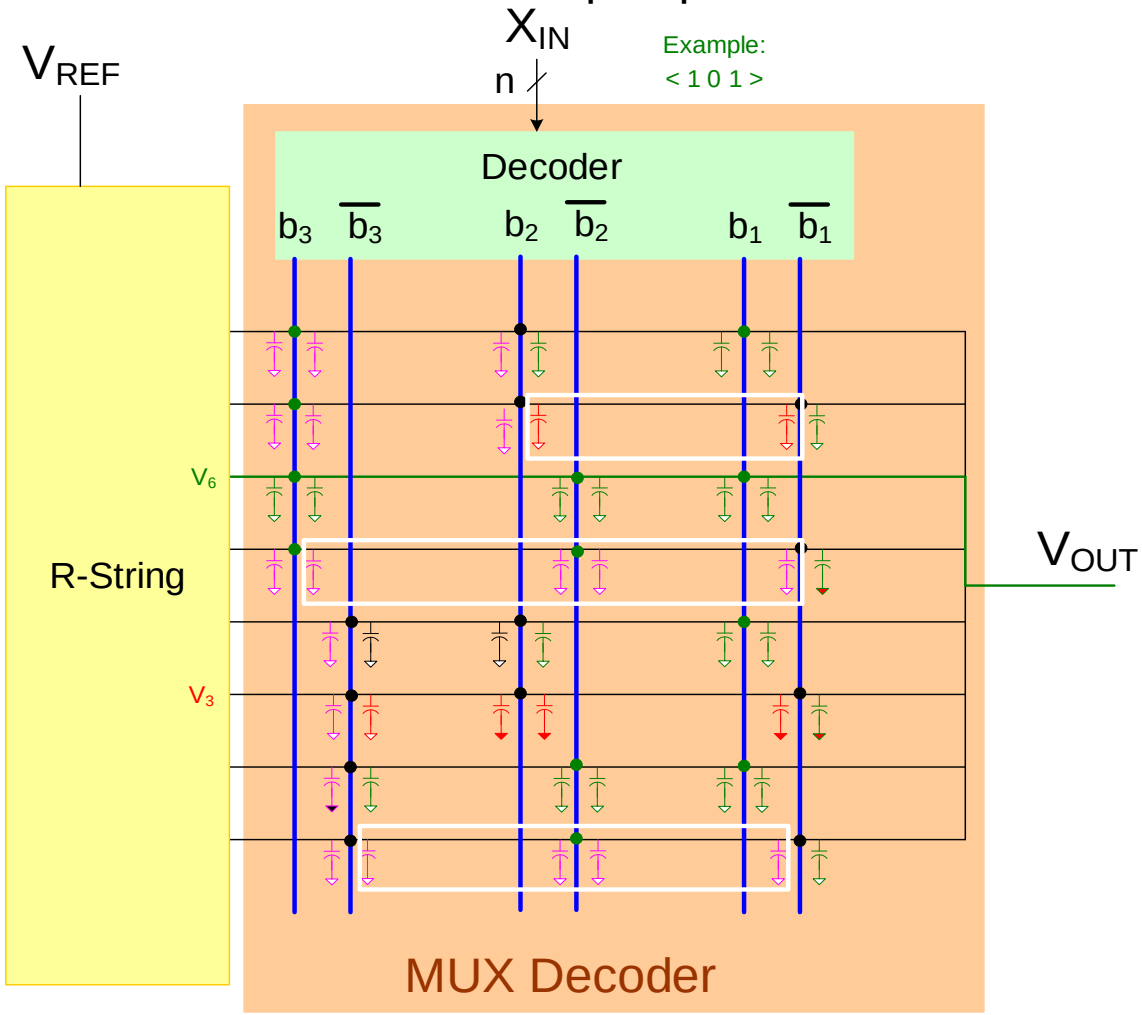
Assume all C's initially with 0V

Red denotes V_3, green denotes V_6, black denotes 0V, Purple some other voltage

R-String DAC

Transition from <010> to <101>

White boxes show capacitors dependent upon previous code <010>

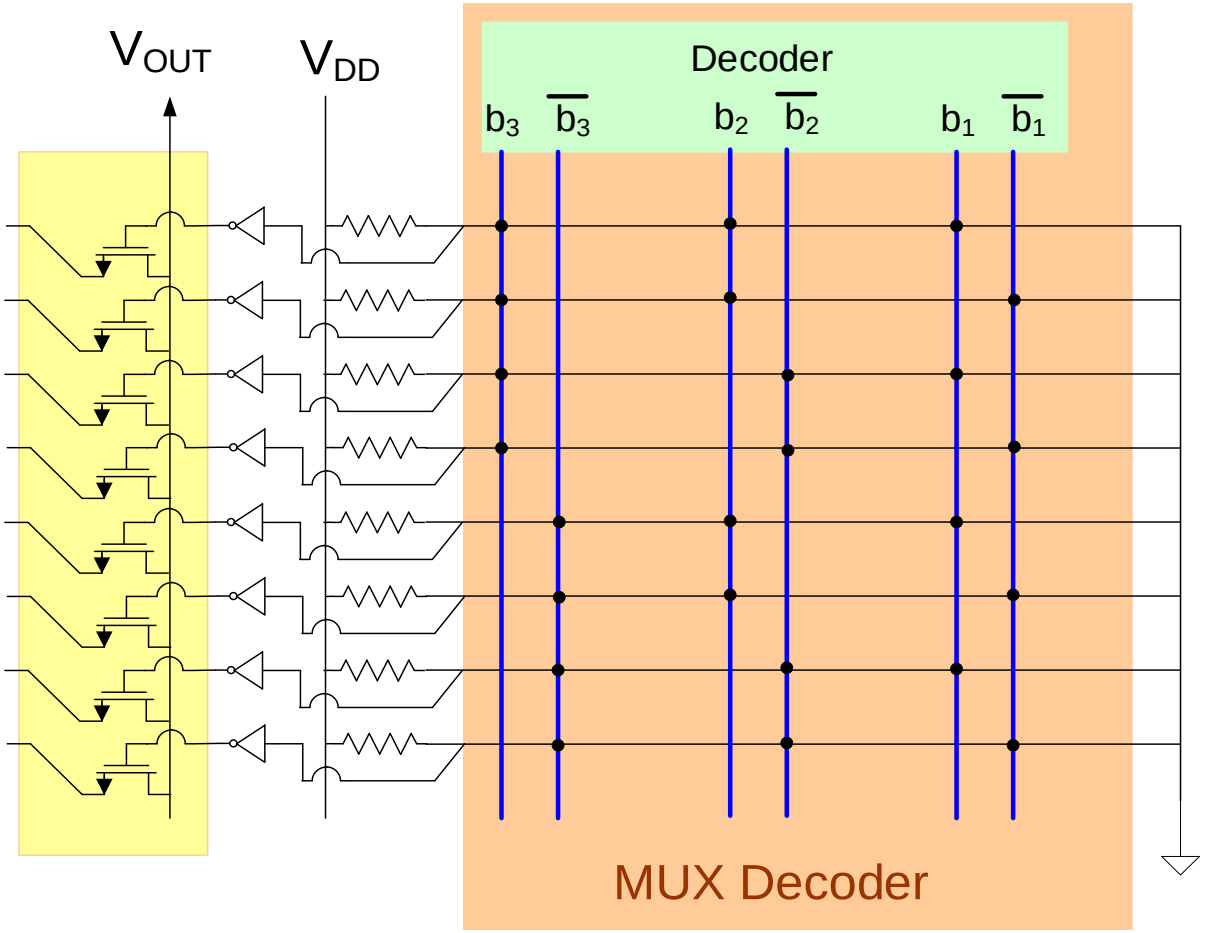


Previous-Code Dependent Settling

Assume all C's initially with 0V

Red denotes V_3, green denotes V_6, black denotes 0V, Purple some other voltage

R-String DAC



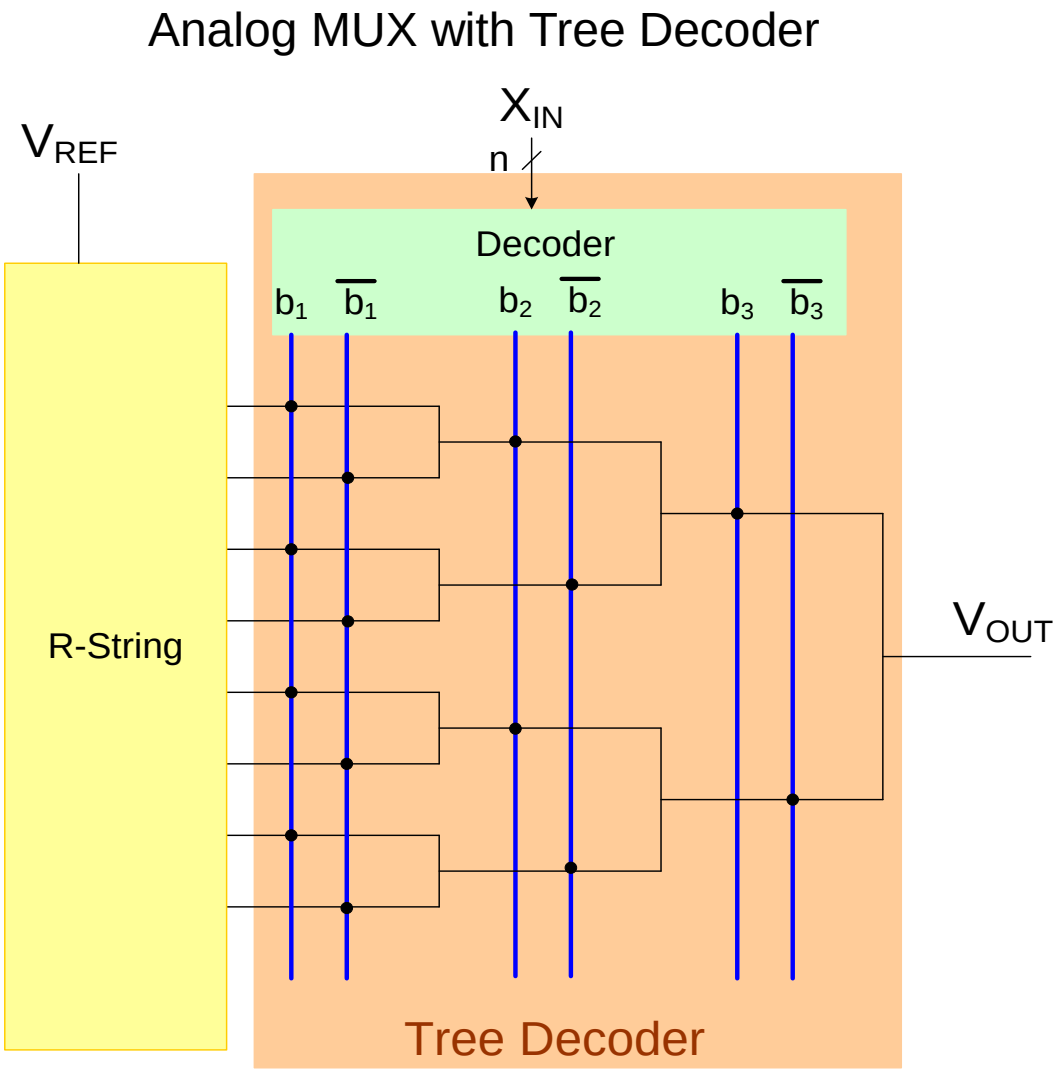
MUX-Decoder in Digital Domain

Single transistor used at each marked intersection to form PTL -NAND gates

Do the resistors that form part of PTL dissipate any substantial power?

No because only one will be conducting for any DAC output

R-String DAC


Analog MUX with Tree Decoder
V_{REF}
X_{IN}
n
Decoder
b_1 $\overline{b_1}$ b_2 $\overline{b_2}$ b_3 $\overline{b_3}$
R-String
V_{OUT}
Tree Decoder

Stay Safe and Stay Healthy !

End of Lecture 32